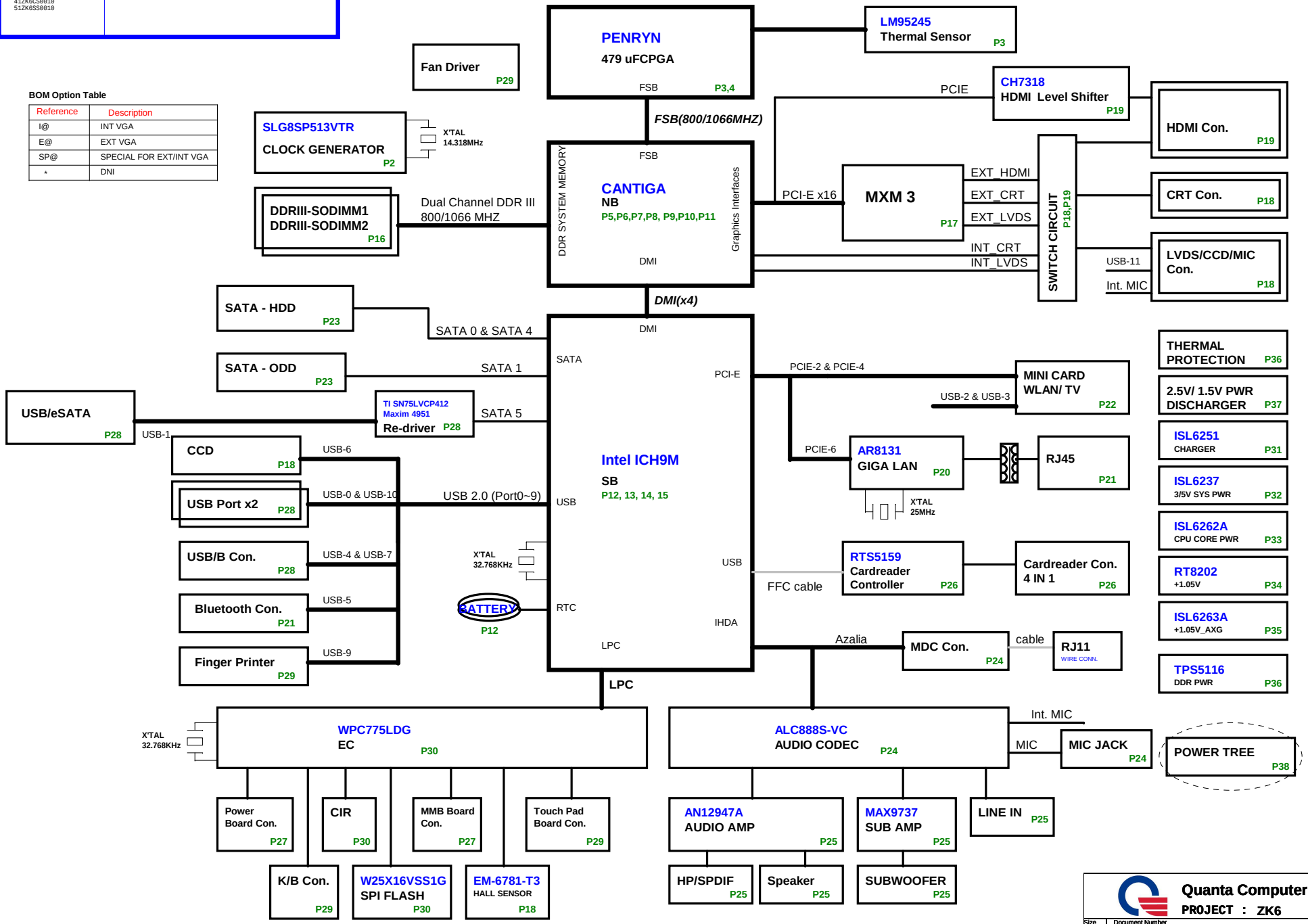
VER : 1A

BOM P/N	Description
31ZK6MB0000 41ZK6CS0000 51ZK6SS0000 31ZK6MB0010 41ZK6CS0010 51ZK6SS0010	uma / mxm 00 / 10

ZK6 MB Block Diagram

BOM Option Table

Reference	Description
I@	INT VGA
E@	EXT VGA
SP@	SPECIAL FOR EXT/INT VGA
*	DNI



Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	Block Diagram	1A

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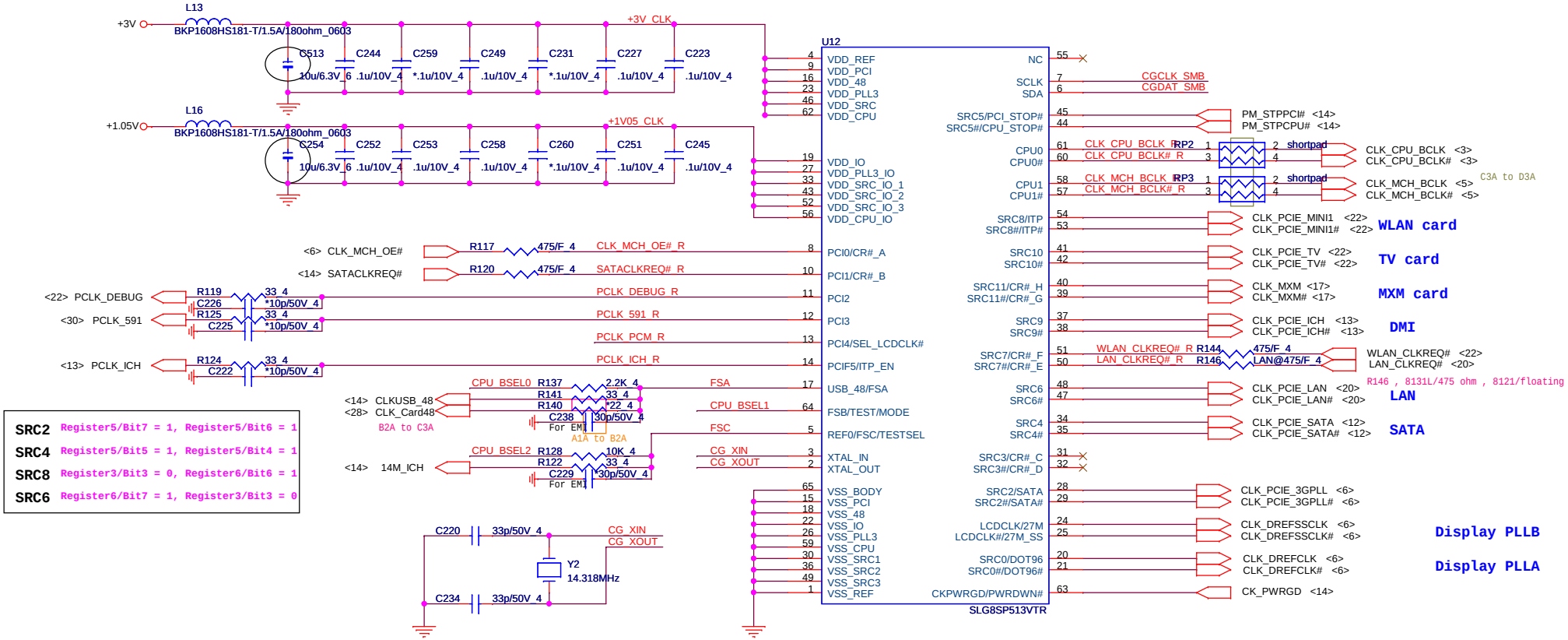
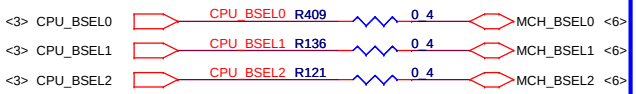
Clock Generator

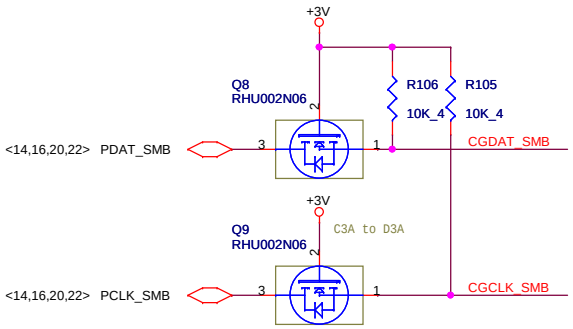


SRC2	Register5/Bit7 = 1, Register5/Bit6 = 1
SRC4	Register5/Bit5 = 1, Register5/Bit4 = 1
SRC8	Register3/Bit3 = 0, Register6/Bit6 = 1
SRC6	Register6/Bit7 = 1, Register3/Bit3 = 0

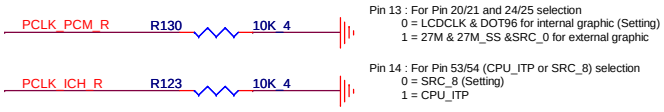
CPU Clock select



FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz



Clock Generator Strap table



Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	CLOCK GENERATOR	1A

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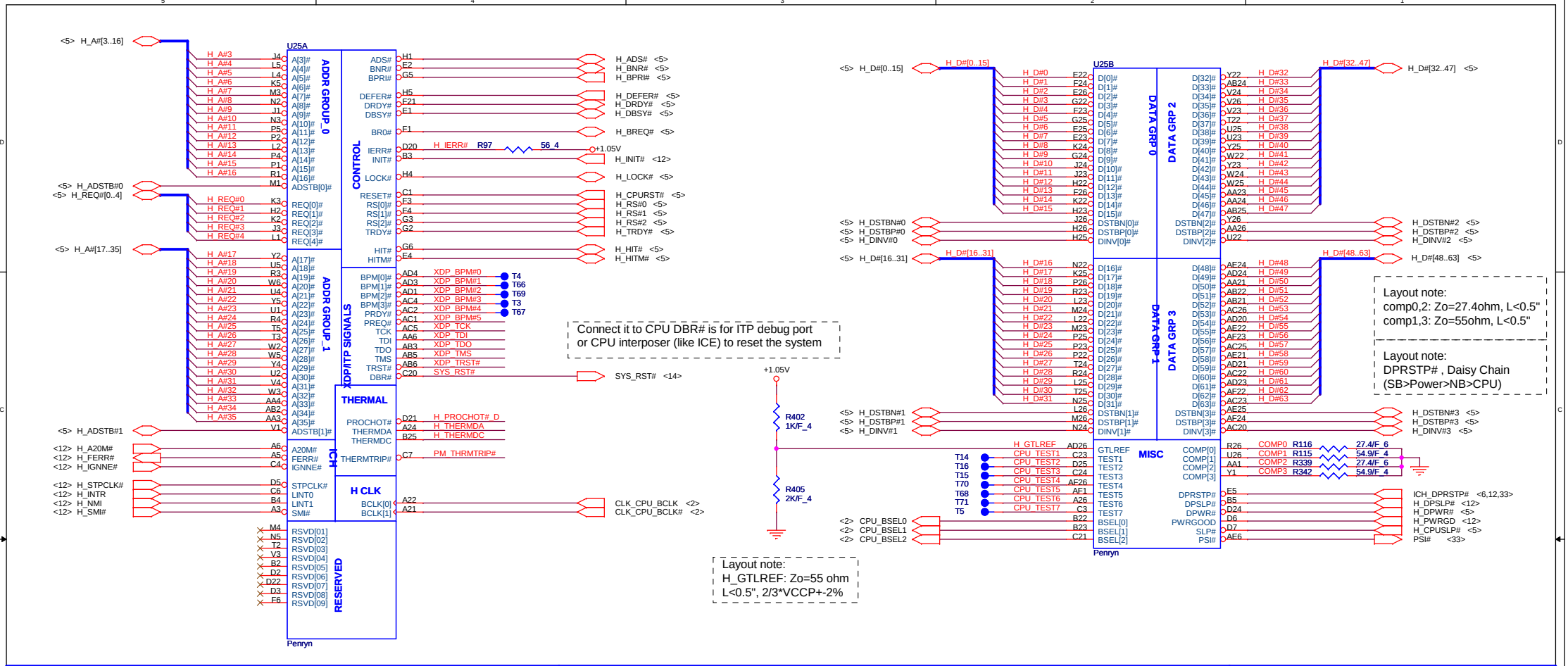
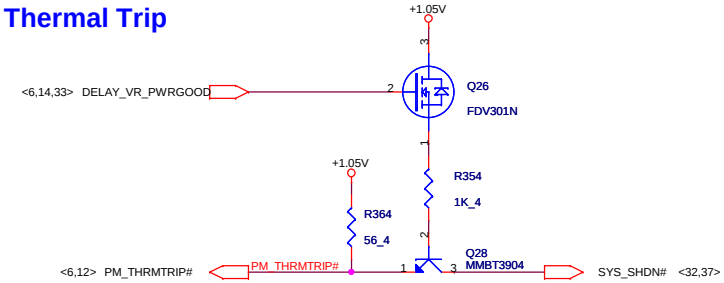


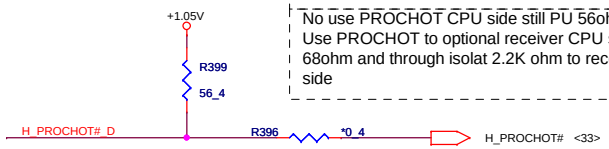
Thermal Trip



Processor hot

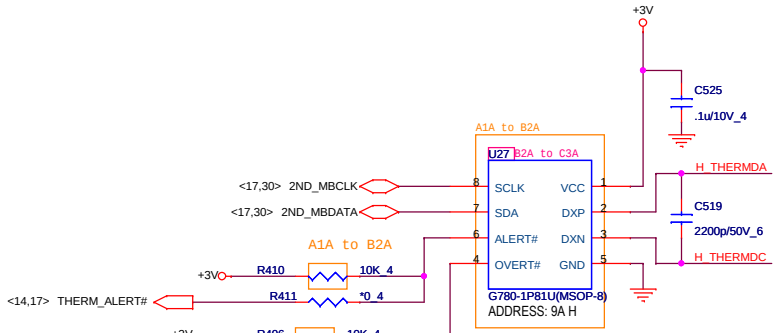
No use Thermal trip CPU side still PU 56ohm. Use Thermal trip can share PU at SB side

No use PROCHOT CPU side still PU 56ohm. Use PROCHOT to optional receiver CPU side PU 68ohm and through isolat 2.2K ohm to receiver side



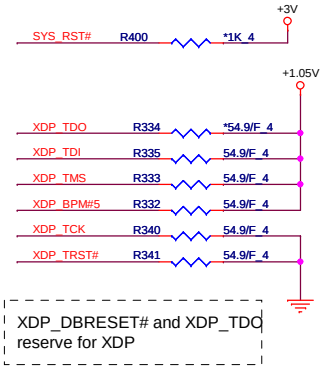
CPU 1/2

CPU Thermal monitor



NS	none
WINDBOND	AL83L771K02
GMT	AL000780003

XDP PU/PD



XDP_DBRESET# and XDP_TDO reserve for XDP

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	CPU Host Bus	1A

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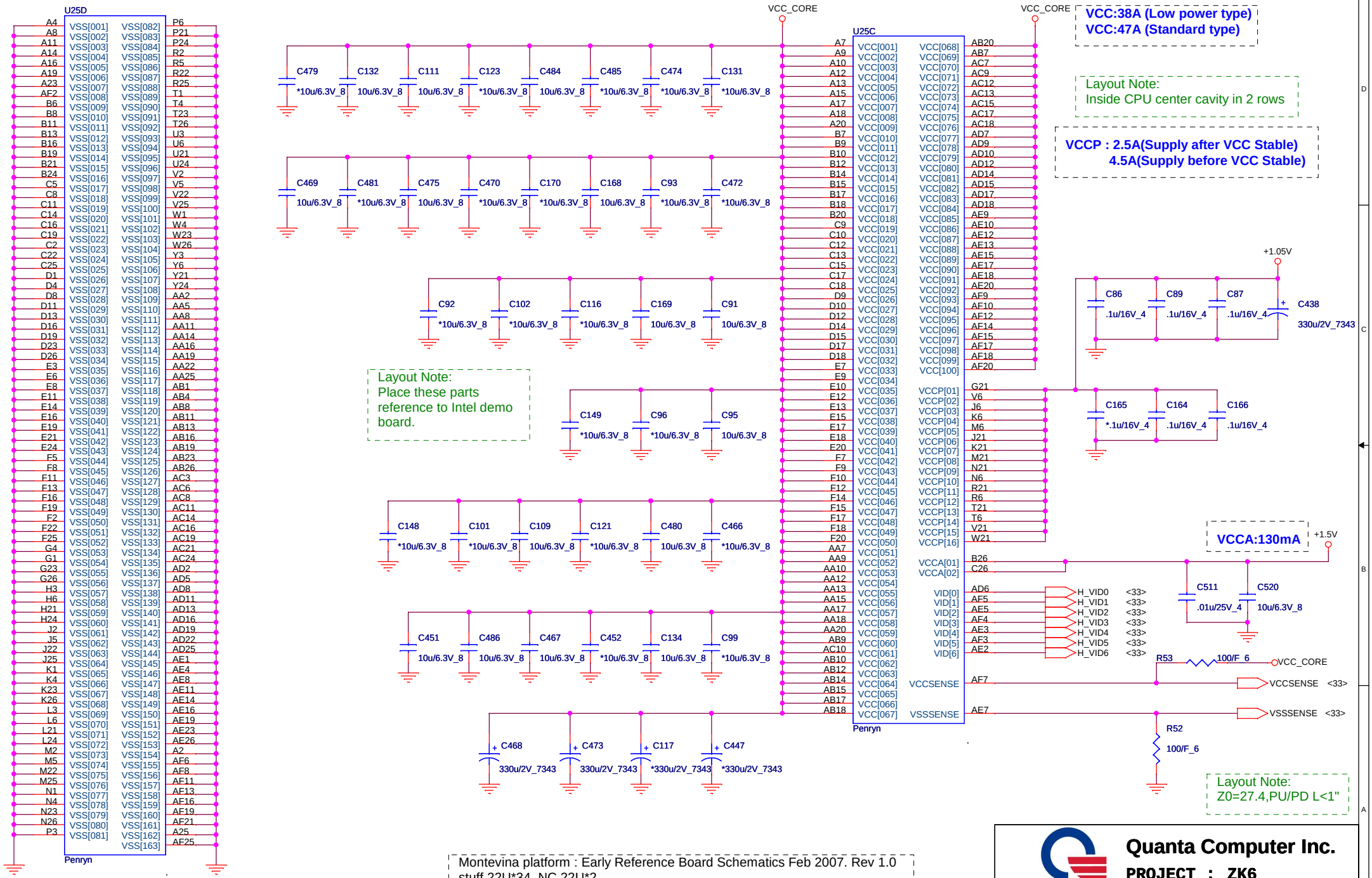

CPU 2/2

Montevina platform : Early Reference Board Schematics Feb 2007. Rev 1.0
stuff 22U*34, NC 22U*2
stuff 330U*2, NC330U*2

Quanta Computer Inc.

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	CPU Power	1A

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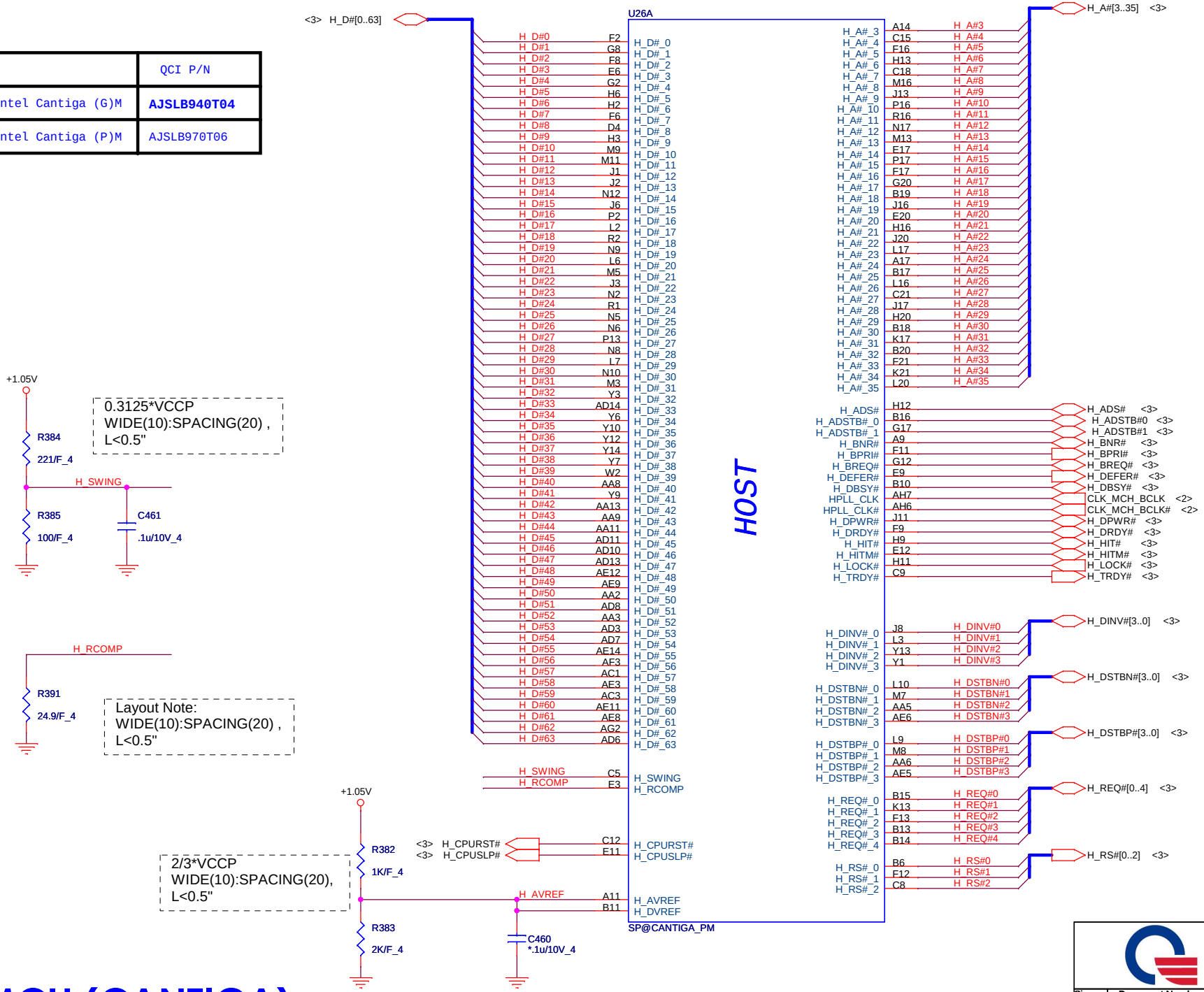
	QCI P/N
Intel Cantiga (G)M	**AJSLB940T04**
Intel Cantiga (P)M	AJSLB970T06



GMCH (CANTIGA)

Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	GMCH HOST	1A

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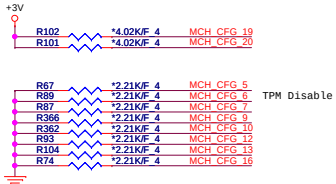
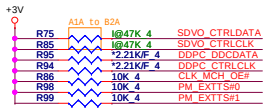
IV@
EV@

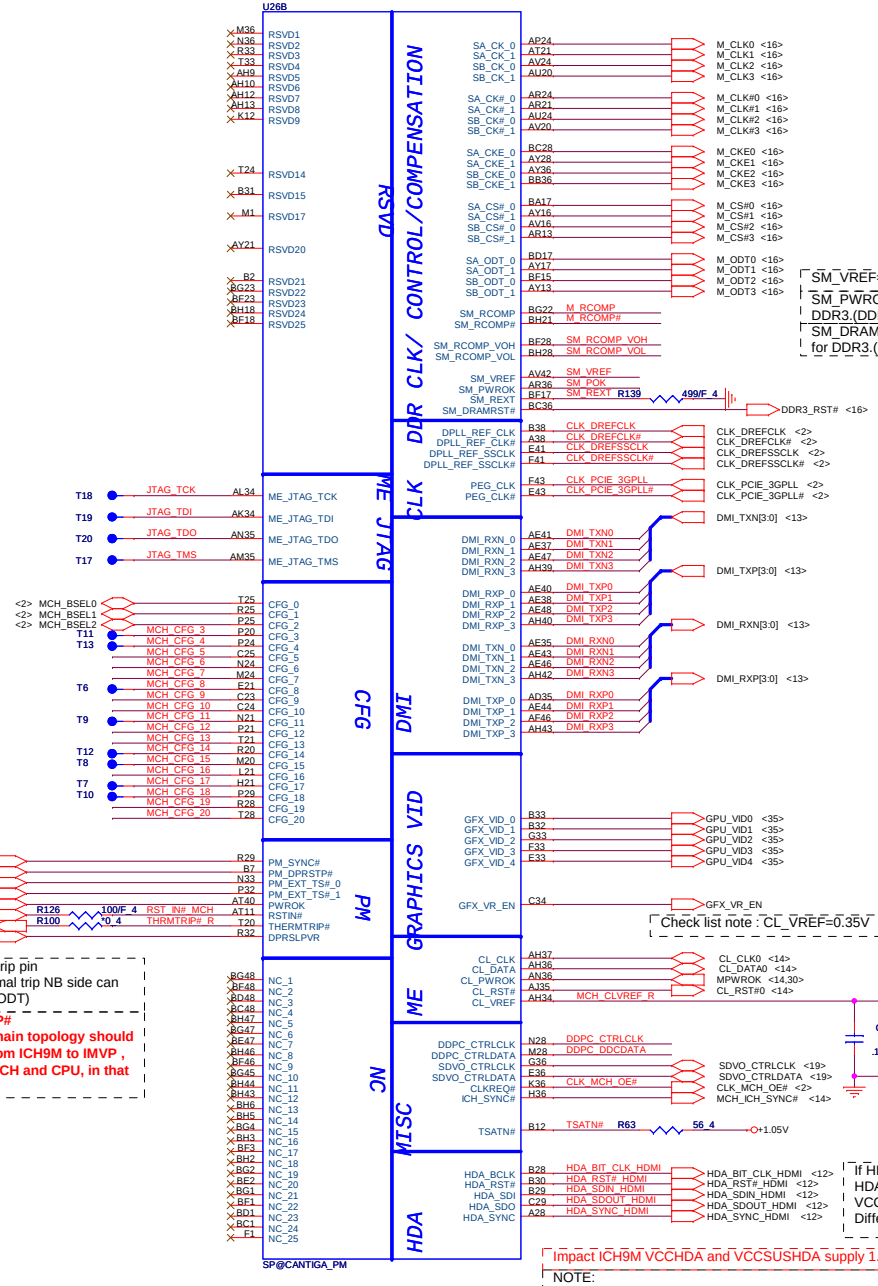
Strap table

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000= FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ mode enable	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR mode enable	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

Strap pin







NB Thermal trip pin
No use Thermal trip NB side can NC.(NB has ODT)

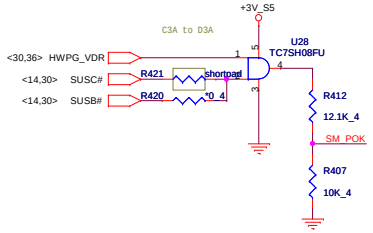
PM_DPRSTP#
The Daisy chain topology should be routed from ICH9M to IMVP , then to (G)MCH and CPU, in that order.

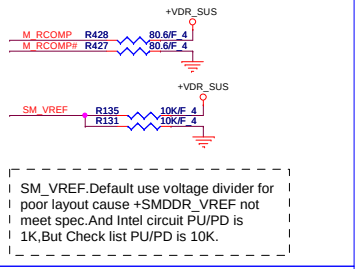
SM_VREF=0.5*VCC_SM

SM_PWROK only for DDR3.(DDR2 PD only)
SM_DRAMRST# only for DDR3.(DDR2:NC)

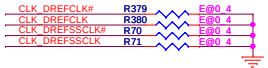
Check list note : CL_VREF=0.35V

DDR3 PWROK

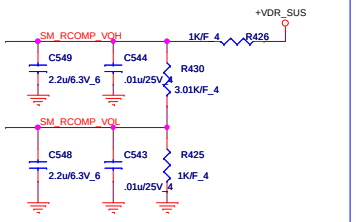




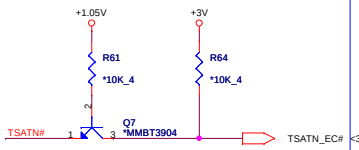
SM_VREF.Default use voltage divider for poor layout cause +SMDDR_VREF not meet spec.And Intel circuit PU/PD is 1K,But Check list PU/PD is 10K.



INTEL FAE Suggest PD for Ext graphics



NB Thermaltrip



DDPC_CTRL for HDMI port C
SDVO_CTRL for HDMI port B

If HDMI not support
HDA --> NC
VCC_HDA-->GND
Differential signal-->NC

<Checklist ver0.8>
If TSATN# is not used, then it must be terminated with a 56-Ω pull-up resistor to VCCP.

<Pin out check issue>
Cantiga EDS 0.7 change Ball B12 to TSATN# from TSATN

Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

GMCH (CANTIGA)

Quanta Computer Inc.		
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	GMCH DMI	1A
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IV@

EV@

SP@

IV&EV Dis/Enable setting

If LVDS no use,all signal can NC

U26C

<18> L_BKLT_CTRL — L32 L_BKLT_CTRL
<18> INT_LVDS_BLON — G32 L_BKLT_EN
R92 I@10K_4 L_CTRL_CLK — M32 L_CTRL_CLK
+3V — R91 I@10K_4 L_CTRL_DATA — M33 L_CTRL_DATA
<18> INT_LVDS_EDIDCLK — K33 L_DDC_CLK
<18> INT_LVDS_EDIDDATA — J33 L_DDC_DATA
<18> INT_LVDS_DIGON — M29 L_VDD_EN
R65 I@2.37K/F_4 — C44 LVDS_IBG
B43 LVDS_VBG
E37 LVDS_VREFH
E38 LVDS_VREFL
<17> INT_TXLCLKOUT- — INT_TXLCLKOUT- — C41 LVDSA_CLK#
<17> INT_TXLCLKOUT+ — INT_TXLCLKOUT+ — C40 LVDSA_CLK
<17> INT_TXUCLKOUT- — INT_TXUCLKOUT- — B37 LVDSB_CLK#
<17> INT_TXUCLKOUT+ — INT_TXUCLKOUT+ — A37 LVDSB_CLK
<17> INT_TXLOUT0- — INT_TXLOUT0- — H47 LVDSA_DATA#_0
<17> INT_TXLOUT1- — INT_TXLOUT1- — E46 LVDSA_DATA#_1
<17> INT_TXLOUT2- — INT_TXLOUT2- — G40 LVDSA_DATA#_2
A40 LVDSA_DATA#_3
<17> INT_TXLOUT0+ — INT_TXLOUT0+ — H48 LVDSA_DATA_0
<17> INT_TXLOUT1+ — INT_TXLOUT1+ — D45 LVDSA_DATA_1
<17> INT_TXLOUT2+ — INT_TXLOUT2+ — F40 LVDSA_DATA_2
B40 LVDSA_DATA_3
<17> INT_TXUOUT0- — INT_TXUOUT0- — A41 LVDSB_DATA#_0
<17> INT_TXUOUT1- — INT_TXUOUT1- — H38 LVDSB_DATA#_1
<17> INT_TXUOUT2- — INT_TXUOUT2- — G37 LVDSB_DATA#_2
J37 LVDSB_DATA#_3
<17> INT_TXUOUT0+ — INT_TXUOUT0+ — B42 LVDSB_DATA_0
<17> INT_TXUOUT1+ — INT_TXUOUT1+ — G38 LVDSB_DATA_1
<17> INT_TXUOUT2+ — INT_TXUOUT2+ — F37 LVDSB_DATA_2
K37 LVDSB_DATA_3

LVDS

R68 75_4 — INT_TV_COMP — F25 TVA_DAC
R69 75_4 — INT_TV_Y/G — H25 TVB_DAC
R84 75_4 — INT_TV_C/R — K25 TVC_DAC
H24 TV_RTN
C31 TV_DCONSEL_0
E32 TV_DCONSEL_1

AI

<17> INT_CRT_BLU — INT_CRT_BLU — E28 CRT_BLUE
<17> INT_CRT_GRN — INT_CRT_GRN — G28 CRT_GREEN
<17> INT_CRT_RED — INT_CRT_RED — J28 CRT_RED
G29 CRT_IRTN
<17> INT_CRT_DDCCLK — H32 CRT_DDC_CLK
<17> INT_CRT_DDCDAT — J32 CRT_DDC_DATA
<17> INT_HSYNC — INT_HSYNC — J29 CRT_HSYNC
CRTIREF — E29 CRT_TVO_IREF
<17> INT_VSYNC — INT_VSYNC — L29 CRT_VSYNC

VGA

SP@CANTIGA_PM

PCI-EXPRESS GRAPHICS

L<0.5" , If PCIE not support still connect to +VCC_PEG

+1.05V

PEG_COMPI — T37 EXP_A_COMPX — R103 49.9/F_4
PEG_COMPO — T36

PEG_RX#_0 — H44 PEG_RXN0
PEG_RX#_1 — J46 PEG_RXN1
PEG_RX#_2 — L44 PEG_RXN2
PEG_RX#_3 — L40 PEG_RXN3
PEG_RX#_4 — N41 PEG_RXN4
PEG_RX#_5 — P48 PEG_RXN5
PEG_RX#_6 — N44 PEG_RXN6
PEG_RX#_7 — T43 PEG_RXN7
PEG_RX#_8 — U43 PEG_RXN8
PEG_RX#_9 — Y43 PEG_RXN9
PEG_RX#_10 — Y48 PEG_RXN10
PEG_RX#_11 — Y36 PEG_RXN11
PEG_RX#_12 — AA43 PEG_RXN12
PEG_RX#_13 — AD37 PEG_RXN13
PEG_RX#_14 — AC47 PEG_RXN14
PEG_RX#_15 — AD39 PEG_RXN15
PEG_RXN[15:0] <17>

PEG_RX_0 — H43 PEG_RXP0
PEG_RX_1 — J44 PEG_RXP1
PEG_RX_2 — L43 PEG_RXP2
PEG_RX_3 — L41 PEG_RXP3
PEG_RX_4 — N40 PEG_RXP4
PEG_RX_5 — P47 PEG_RXP5
PEG_RX_6 — N43 PEG_RXP6
PEG_RX_7 — T42 PEG_RXP7
PEG_RX_8 — U42 PEG_RXP8
PEG_RX_9 — Y42 PEG_RXP9
PEG_RX_10 — W47 PEG_RXP10
PEG_RX_11 — Y37 PEG_RXP11
PEG_RX_12 — AA42 PEG_RXP12
PEG_RX_13 — AD36 PEG_RXP13
PEG_RX_14 — AC48 PEG_RXP14
PEG_RX_15 — AD40 PEG_RXP15
PEG_RXP[15:0] <17>

PEG_TX#_0 — J41 C_PEG_TXN0 — C103 — .1u/10V_4 — PEG_TXN0
PEG_TX#_1 — M46 C_PEG_TXN1 — C119 — .1u/10V_4 — PEG_TXN1
PEG_TX#_2 — M47 C_PEG_TXN2 — C125 — .1u/10V_4 — PEG_TXN2
PEG_TX#_3 — M40 C_PEG_TXN3 — C133 — .1u/10V_4 — PEG_TXN3
PEG_TX#_4 — M42 C_PEG_TXN4 — C105 — E@.1u/10V_4 — PEG_TXN4
PEG_TX#_5 — R48 C_PEG_TXN5 — C141 — E@.1u/10V_4 — PEG_TXN5
PEG_TX#_6 — N38 C_PEG_TXN6 — C154 — E@.1u/10V_4 — PEG_TXN6
PEG_TX#_7 — T40 C_PEG_TXN7 — C186 — E@.1u/10V_4 — PEG_TXN7
PEG_TX#_8 — U37 C_PEG_TXN8 — C197 — E@.1u/10V_4 — PEG_TXN8
PEG_TX#_9 — U40 C_PEG_TXN9 — C201 — E@.1u/10V_4 — PEG_TXN9
PEG_TX#_10 — Y40 C_PEG_TXN10 — C211 — E@.1u/10V_4 — PEG_TXN10
PEG_TX#_11 — AA46 C_PEG_TXN11 — C215 — E@.1u/10V_4 — PEG_TXN11
PEG_TX#_12 — AA37 C_PEG_TXN12 — C208 — E@.1u/10V_4 — PEG_TXN12
PEG_TX#_13 — AA40 C_PEG_TXN13 — C230 — E@.1u/10V_4 — PEG_TXN13
PEG_TX#_14 — AD43 C_PEG_TXN14 — C237 — E@.1u/10V_4 — PEG_TXN14
PEG_TX#_15 — AC46 C_PEG_TXN15 — C239 — E@.1u/10V_4 — PEG_TXN15
PEG_TXN[15:0] <17>

PEG_TX_0 — J42 C_PEG_TXP0 — C100 — .1u/10V_4 — PEG_TXP0
PEG_TX_1 — L46 C_PEG_TXP1 — C113 — .1u/10V_4 — PEG_TXP1
PEG_TX_2 — M48 C_PEG_TXP2 — C122 — .1u/10V_4 — PEG_TXP2
PEG_TX_3 — M39 C_PEG_TXP3 — C130 — .1u/10V_4 — PEG_TXP3
PEG_TX_4 — M43 C_PEG_TXP4 — C112 — E@.1u/10V_4 — PEG_TXP4
PEG_TX_5 — R47 C_PEG_TXP5 — C147 — E@.1u/10V_4 — PEG_TXP5
PEG_TX_6 — N37 C_PEG_TXP6 — C151 — E@.1u/10V_4 — PEG_TXP6
PEG_TX_7 — T39 C_PEG_TXP7 — C184 — E@.1u/10V_4 — PEG_TXP7
PEG_TX_8 — U36 C_PEG_TXP8 — C194 — E@.1u/10V_4 — PEG_TXP8
PEG_TX_9 — U39 C_PEG_TXP9 — C199 — E@.1u/10V_4 — PEG_TXP9
PEG_TX_10 — Y39 C_PEG_TXP10 — C202 — E@.1u/10V_4 — PEG_TXP10
PEG_TX_11 — Y46 C_PEG_TXP11 — C213 — E@.1u/10V_4 — PEG_TXP11
PEG_TX_12 — AA36 C_PEG_TXP12 — C207 — E@.1u/10V_4 — PEG_TXP12
PEG_TX_13 — AA39 C_PEG_TXP13 — C221 — E@.1u/10V_4 — PEG_TXP13
PEG_TX_14 — AD42 C_PEG_TXP14 — C232 — E@.1u/10V_4 — PEG_TXP14
PEG_TX_15 — AD46 C_PEG_TXP15 — C243 — E@.1u/10V_4 — PEG_TXP15
PEG_TXP[15:0] <17>

IV&EV Dis/Enable setting

<5/31>Montevina_Schematics_Checklist_Rev0_8
a)For TVOUT Disabled, TV_DCONSEL[1:0] Connect to GND. But design guide Rev0.7 show NC.What is correct.
b)For CRT DAC Disable, CRT_DDC_CLK, CRT_DDC_DATA . CRT_HSYNC, CRT_VSYNCThese signals should be connected to GND. But design guide Rev0.7 show NC, Intel suggest follow Design guide.

<check list>	<check list>
For EV@	For IV@
CRT R/G/B 0ohm to GND	CRT R/G/B 150ohm to GND
CRTIREF 0ohm to GND	CRTIREF 976 ohm to GND (>12")

CRTIREF
For IV: 1.02Kohm
For EV:0ohm

R72 SP@1K/F_4 CRTIREF

SP@

CRT_R/G/B
For IV: 150ohm
For EV:0ohm

R73 SP@150_4 INT_CRT_BLU
R83 SP@150_4 INT_CRT_GRN
R88 SP@150_4 INT_CRT_RED

MXM STUFFED.

INT_HSYNC — R82 E@0_4
INT_VSYNC — R80 E@0_4

CRTIREF pull down for IV cantiga 1.02k ohm/F

Quanta Computer Inc.		
PROJECT : ZK6		
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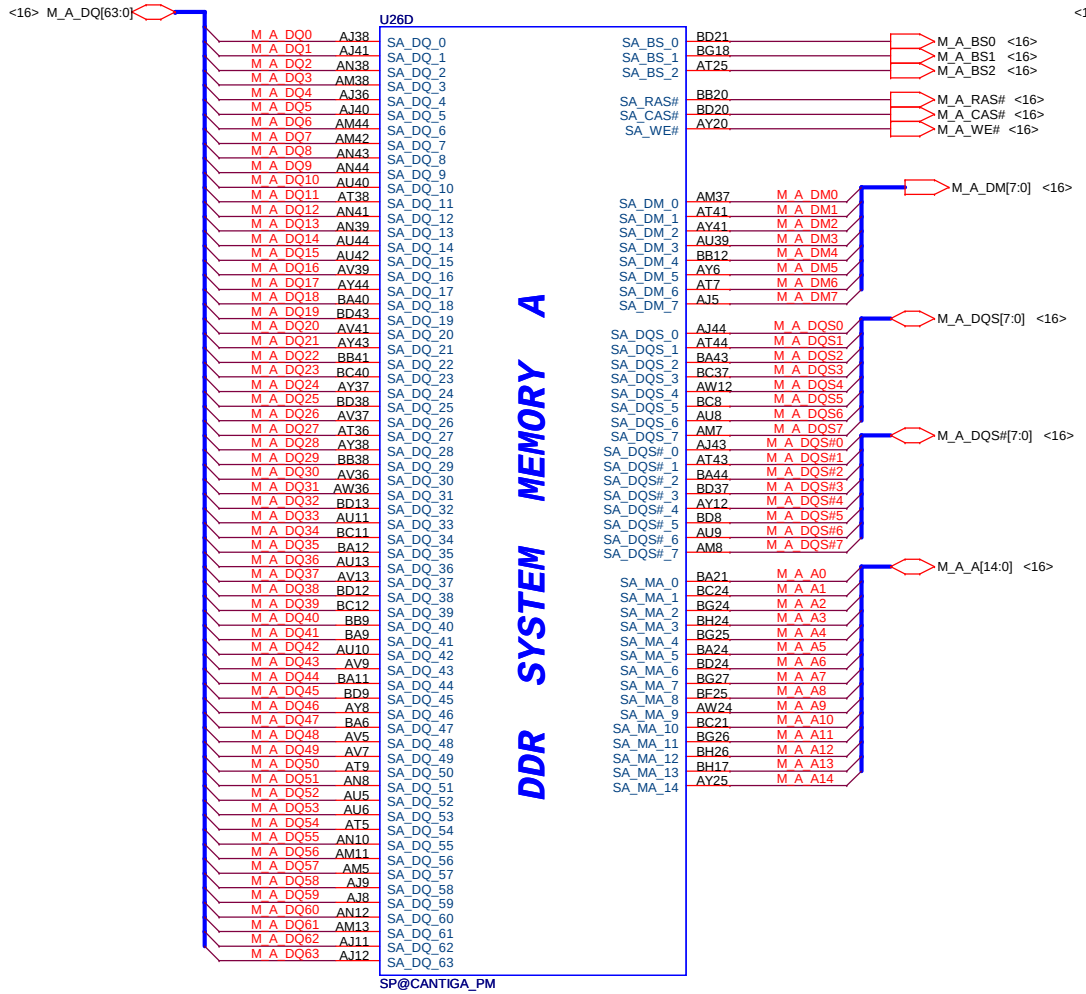
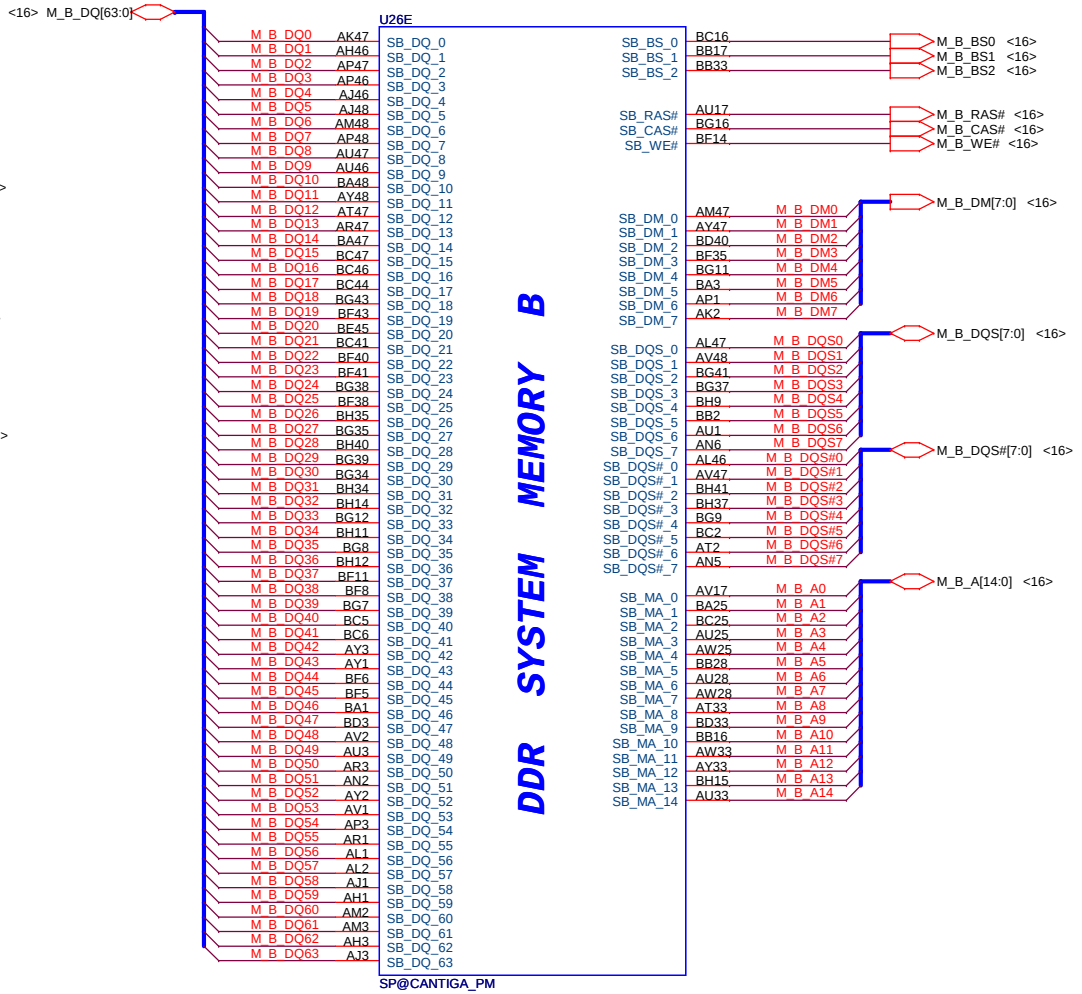




GMCH (CANTIGA)

Quanta Computer Inc.			
PROJECT : ZK6			
Size	Document Number	GMCH DDRIII	Rev 1A
Date: Friday, April 24, 2009	Sheet 8 of 42		

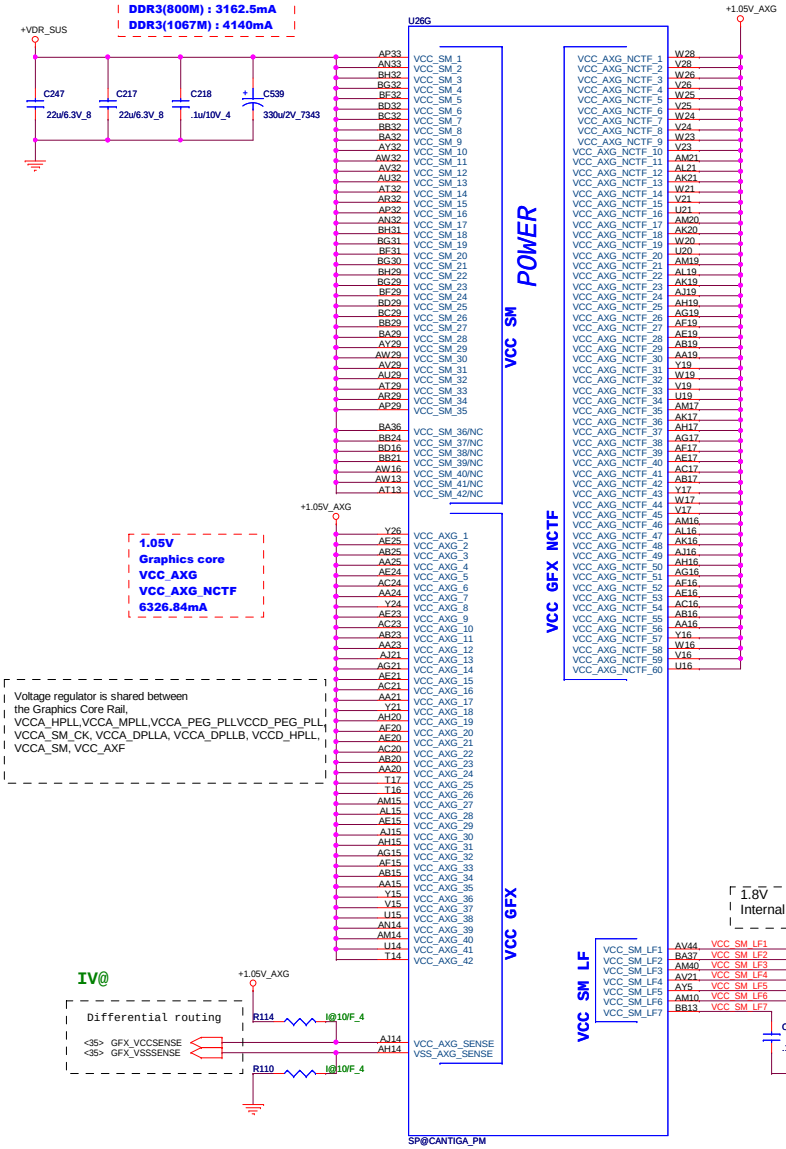
IV@

SP@

VCC_SM(1.5VSUS)
DDR3(800M) : 3162.5mA
DDR3(1067M) : 4140mA

Intel check list(Rev 0.8)
No description for VCC_SM bulk CAP
Intel CRB(Rev 0.7)
330U*1 Reserve near to power
330U*1 near to NB

Intel check list(Rev 0.8)
270U*1 near to power(+V1.05M).
270U*2 near to NB
Intel CRB(Rev 0.7)
270U*3 near to power(+V1.05M).
270U*1 near to NB
ESR=12m ohm

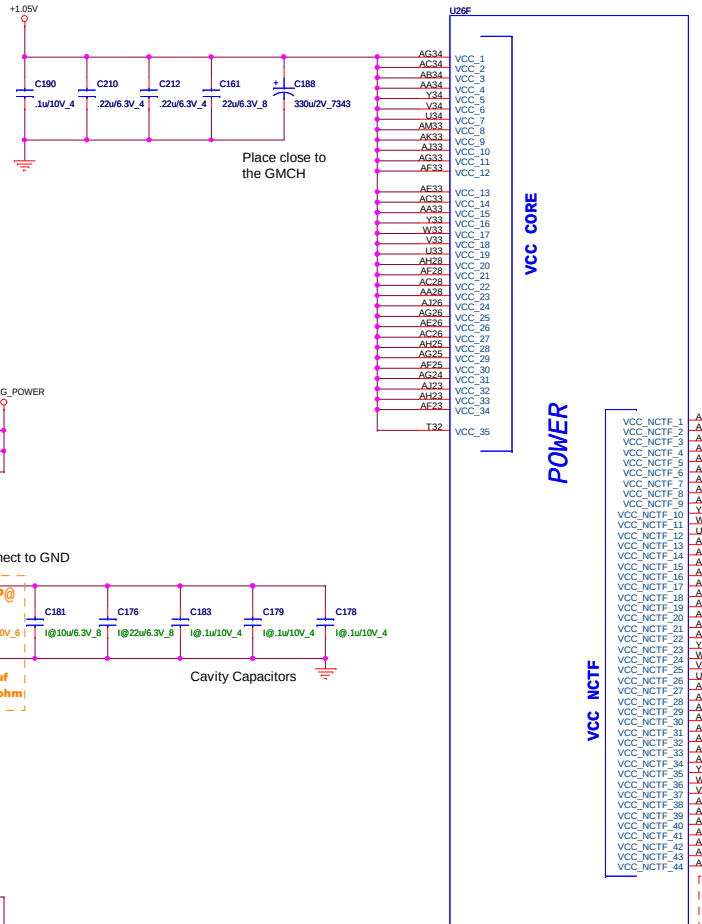


1.05V
Graphics core
VCC_AXG
VCC_AXG_NCTF
6326.84mA

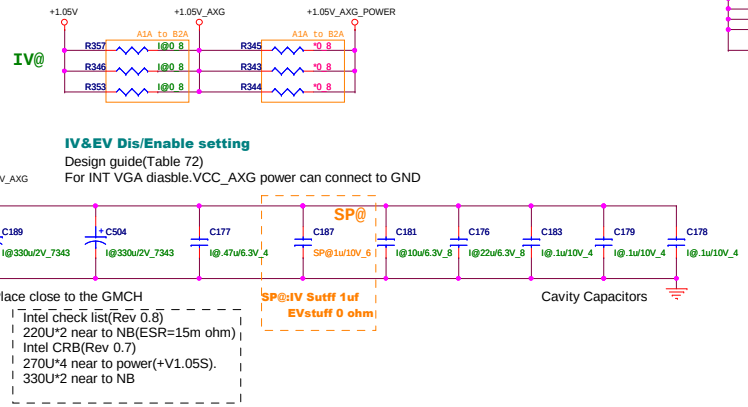
Voltage regulator is shared between the Graphics Core Rail, VCCA_HPLL,VCCA_MPLL,VCCA_PEG_PLLVCCD_PEG_PLL, VCCA_SM_CK, VCCA_DPLLA, VCCA_DPLLB, VCCD_HPLL, VCCA_SM, VCC_AXF

IV@

1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm and VSS_AXG_SENSE PD with 10ohm for Intel suggest



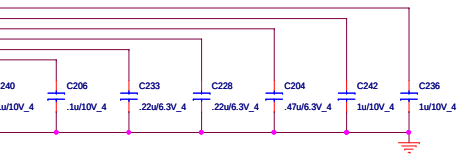
VCC
VCC_NCTF
1210.34mA_EV
1930.4mA_IV
ME Engine
508.12mA
Total Max=2438.52mA



IV&EV Dis/Enable setting
Design guide(Table 72)
For INT VGA diasble.VCC_AXG power can connect to GND

Intel check list(Rev 0.8)
220U*2 near to NB(ESR=15m ohm)
Intel CRB(Rev 0.7)
270U*4 near to power(+V1.05S).
330U*2 near to NB

1.8V
Internal connect to power



GMCH (CANTIGA)

Quanta Computer Inc.
PROJECT : ZK6

Size	Document Number	Rev
	GMCH VCC,NCTF	1A

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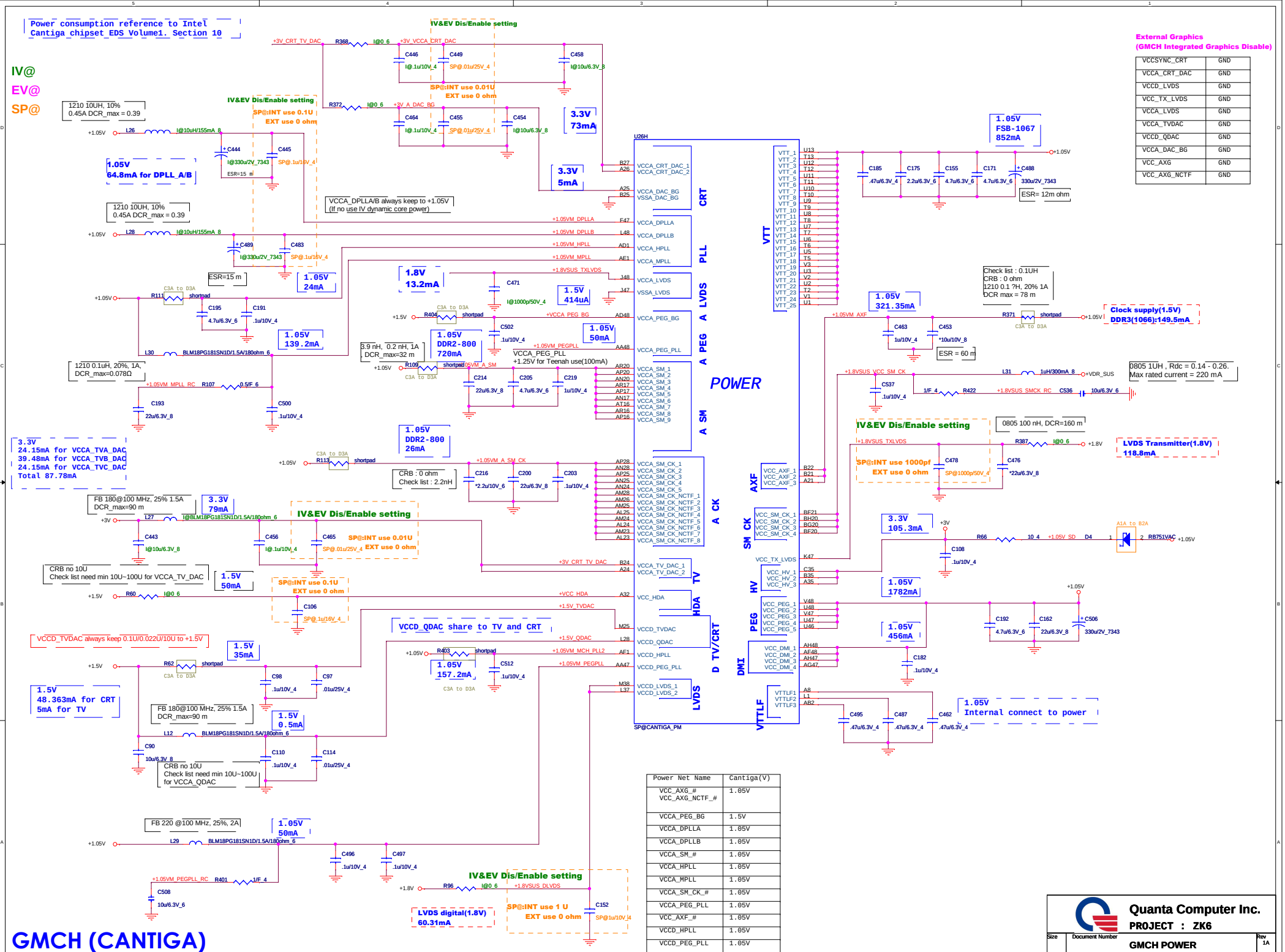
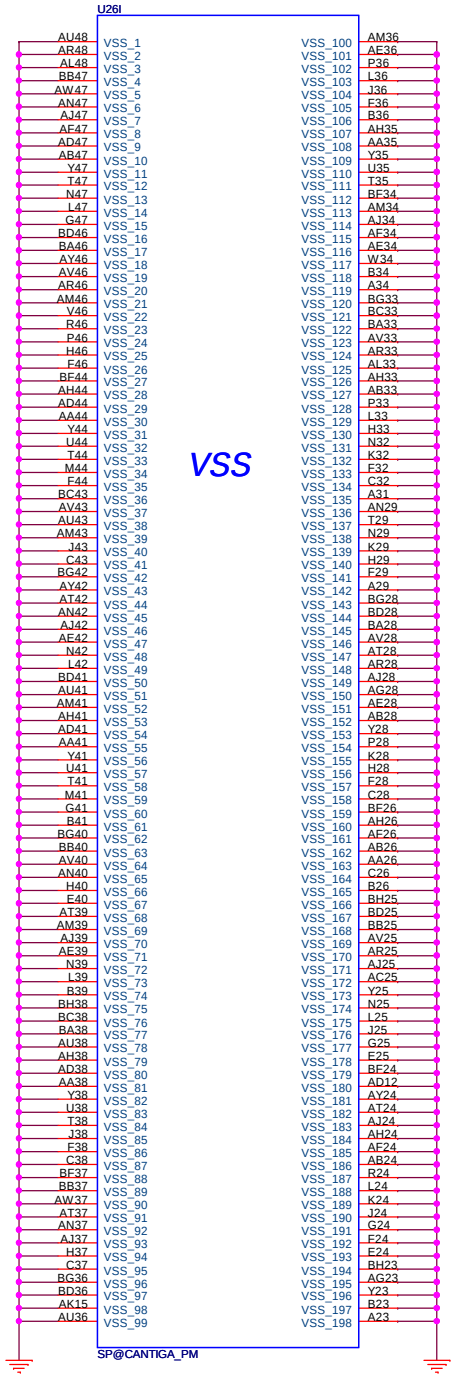


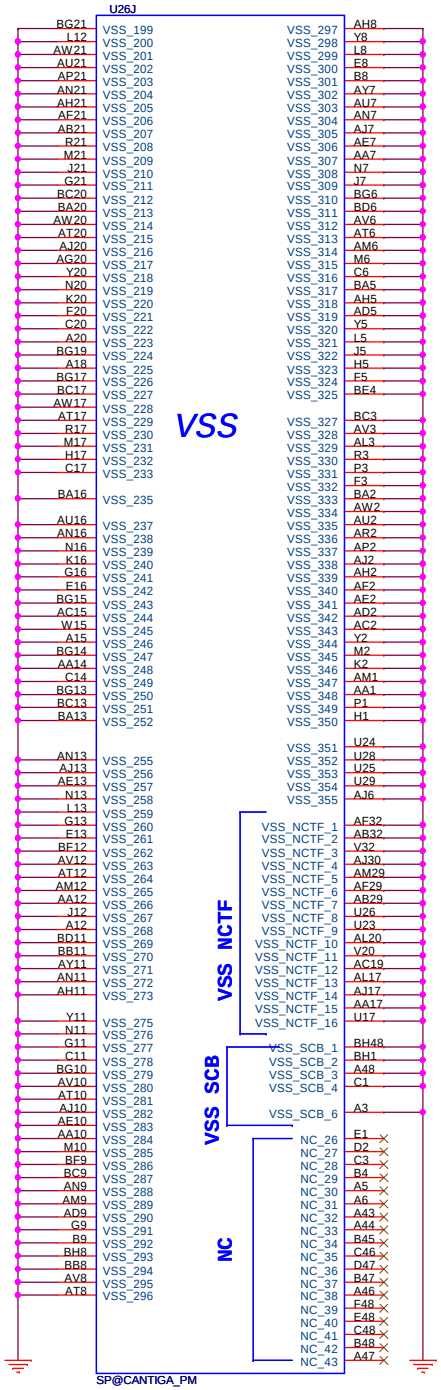
Power Net Name	Cantiga(V)
VCC_AXG_# VCC_AXG_NCTF_#	1.05V
VCCA_PEG_BG	1.5V
VCCA_DPLLA	1.05V
VCCA_DPLLB	1.05V
VCCA_SM_#	1.05V
VCCA_HPLL	1.05V
VCCA_MPLL	1.05V
VCCA_SM_CK_#	1.05V
VCCA_PEG_PLL	1.05V
VCC_AXF_#	1.05V
VCCD_HPLL	1.05V
VCCD_PEG_PLL	1.05V

VCCSYNC_CRT	GND
VCCA_CRT_DAC	GND
VCCD_LVDS	GND
VCC_TX_LVDS	GND
VCCA_LVDS	GND
VCCA_TVDAC	GND
VCCD_QDAC	GND
VCCA_DAC_BG	GND
VCC_AXG	GND
VCC_AXG_NCTF	GND

GMCH (CANTIGA)

Quanta Computer Inc.
PROJECT : ZK6
Size | Document Number | GMCH POWER | Rev 1A
Date: Friday, April 24, 2009 | Sheet 10 of 42





GMCH (CANTIGA)

Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	GMCH VSS	1A

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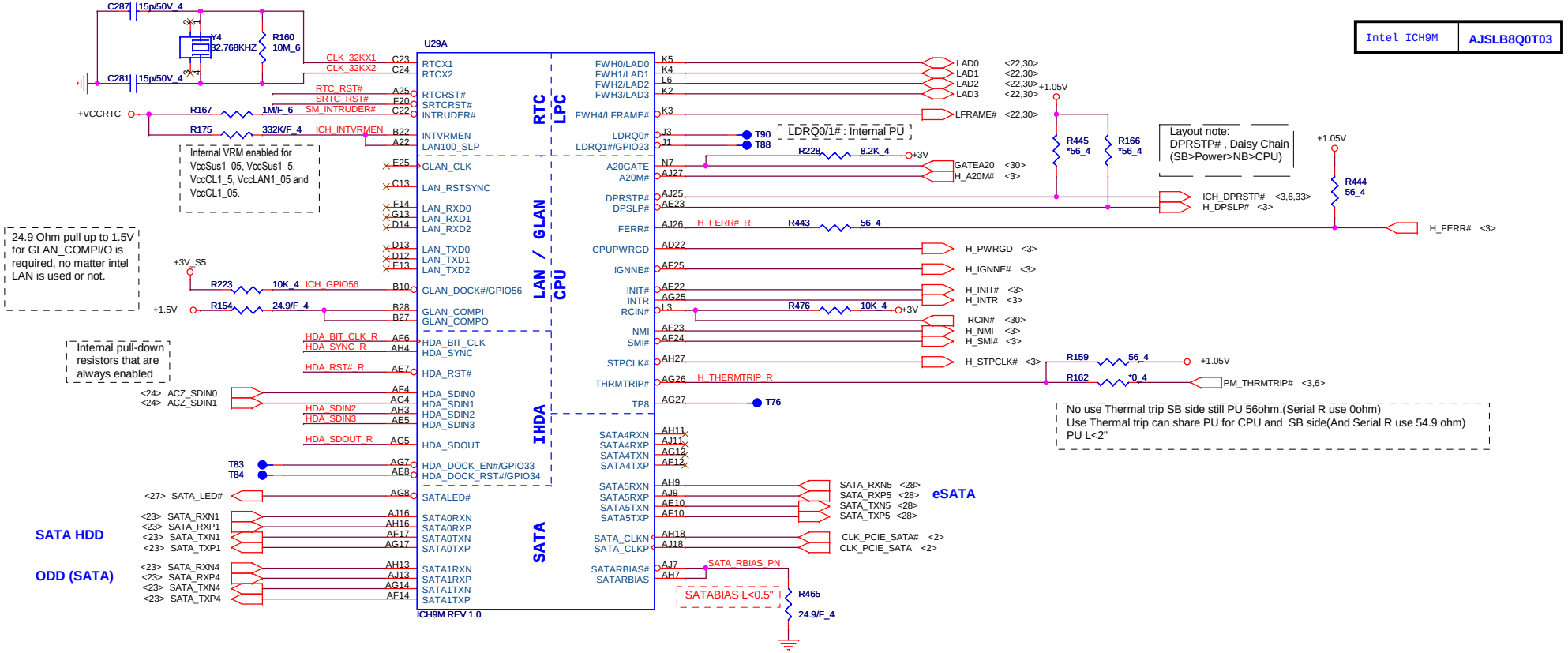
ICH9M

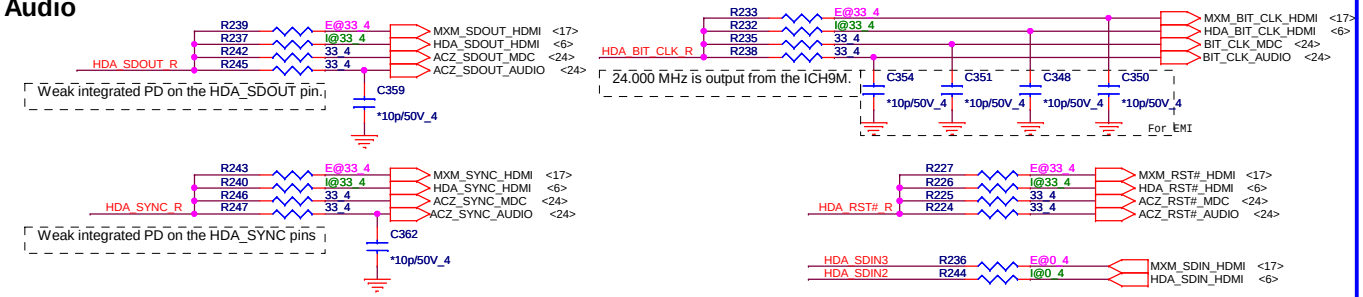
IV@

EV@

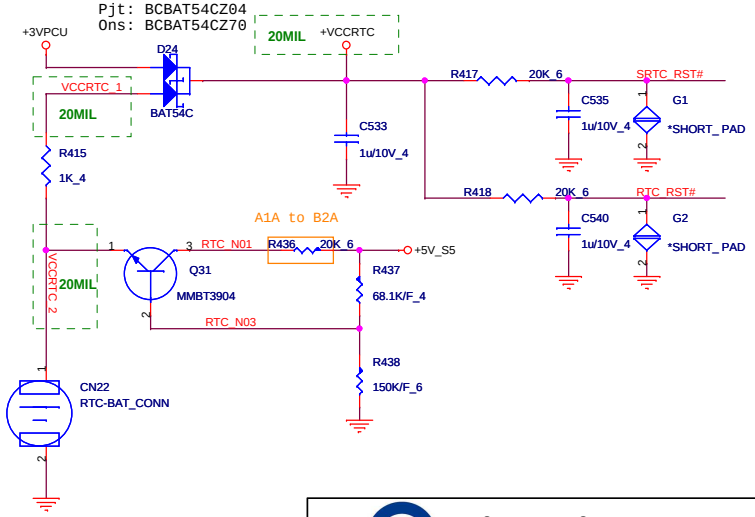
Intel ICH9M	AJSLB8Q0T03



HD Audio



RTC



South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	ICH_TP3 / HDA_SDOUT / Description 0 / 0 / RSVD 0 / 1 / Enter XOR Chain 1 / 0 / Normal opration(Default) 1 / 1 / Set PCIE port config bit 1	<14> ICH_TP3 — ICH_TP3 — R182 *1K_4
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK		HDA_SDOUT_R — R234 *1K_4 — +3V

Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	ICH9M HOST	1A

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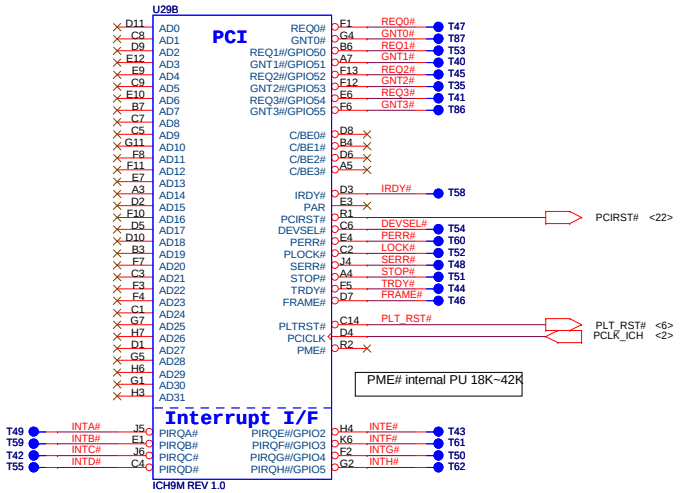
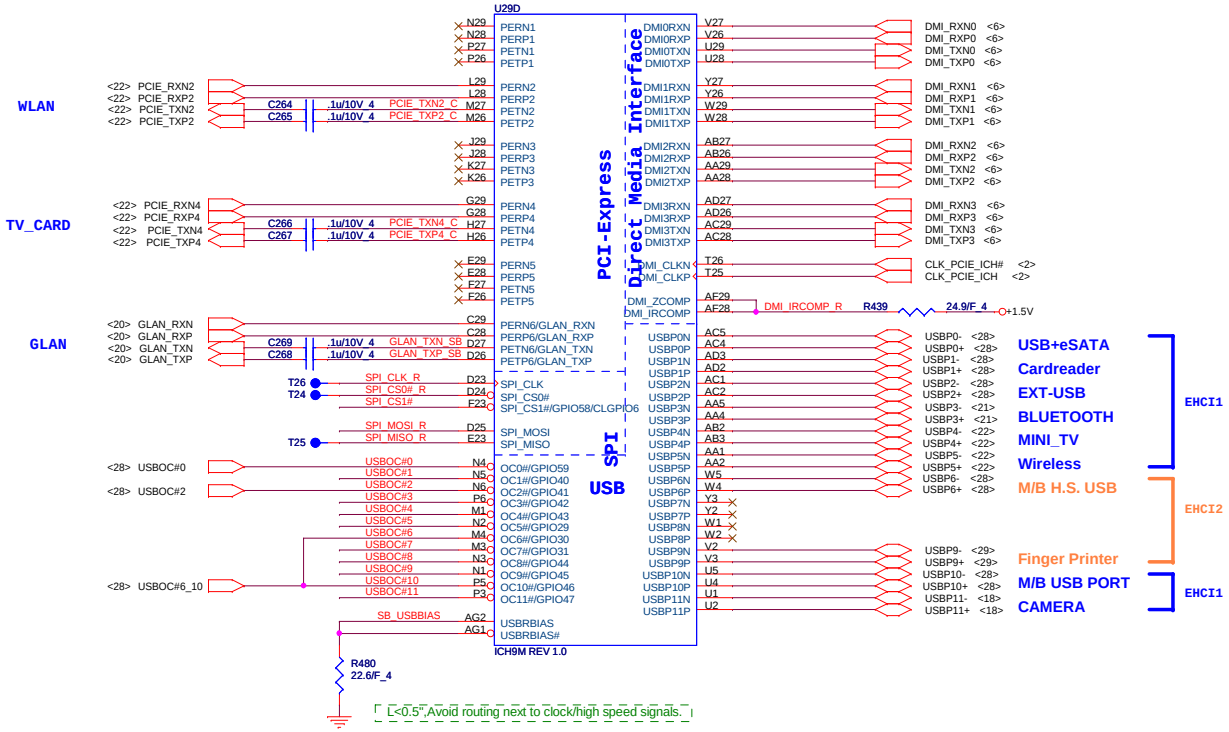
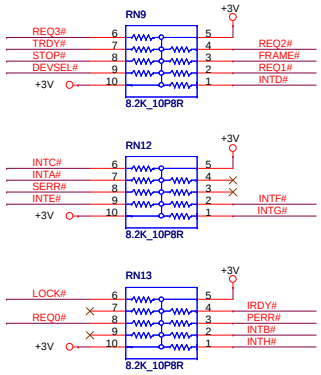
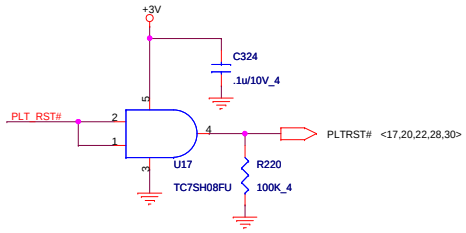
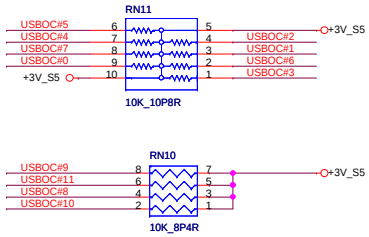
ICH9M





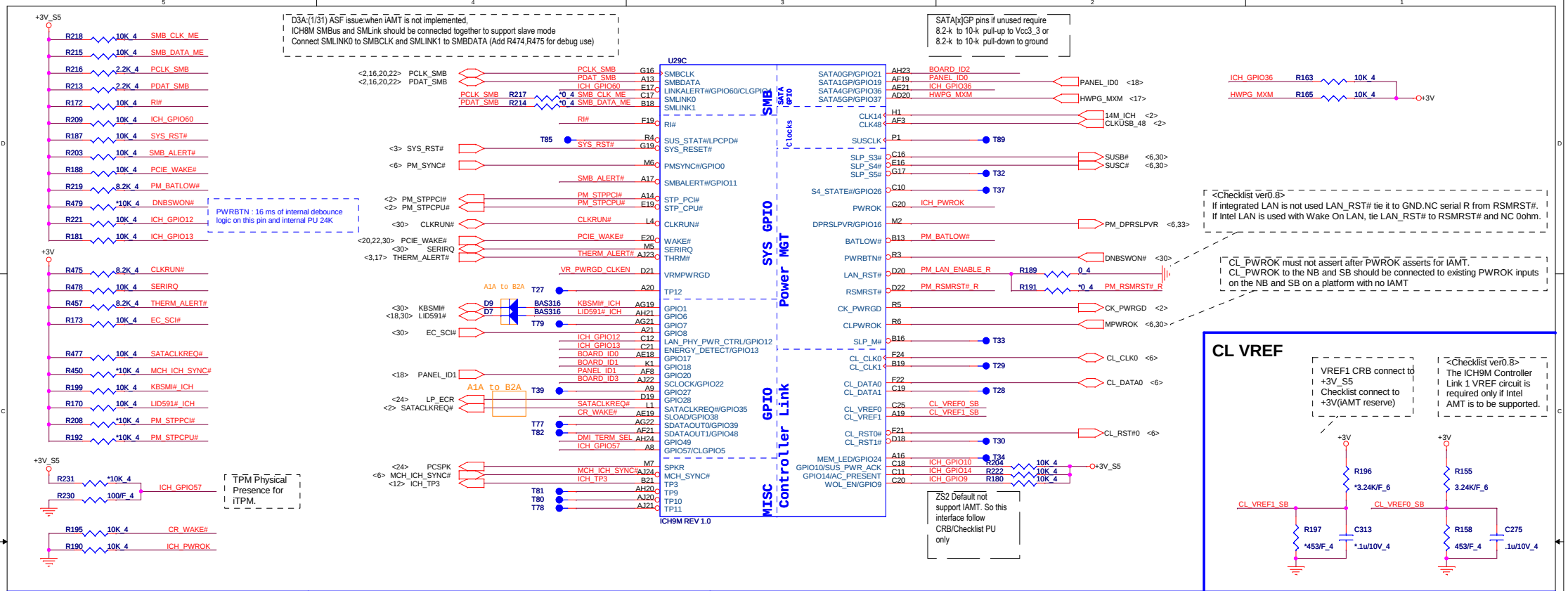






South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R485 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI_R R156 *10K_4 +3V_S5
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0: 0, SPI_CS#1: 1 — Boot Location: SPI PCI_GNT#0: 1, SPI_CS#1: 0 — Boot Location: PCI PCI_GNT#0: 1, SPI_CS#1: 1 — Boot Location: **LPC(Default)**	GNT0# R486 *1K_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK		SPI_CS1# R177 *1K_4

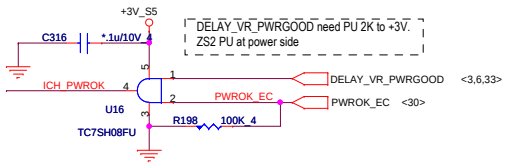


CL VREF

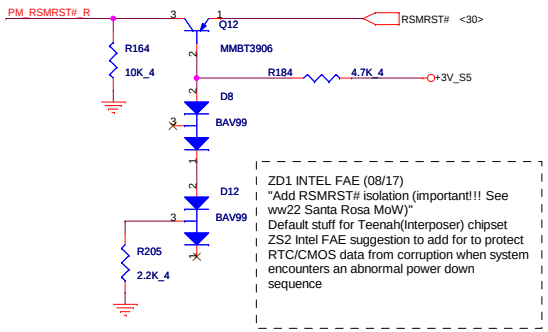
VREF1 CRB connect to +3V_S5
Checklist connect to +3V(iAMT reserve)

<Checklist ver0.8>
The ICH9M Controller Link 1 VREF circuit is required only if Intel AMT is to be supported.

ICH PWROK

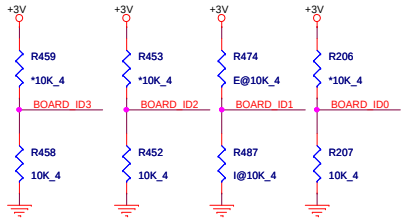


Resume RST



M/B ID

ID0 :: ZK=0 , ZR=1
ID1 :: UMA=0 , MXM=1

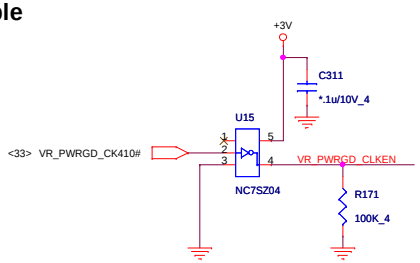


Board ID	ID3	ID2	ID1	ID0
default	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0

South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R229 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R446 *1K_4

CLK Enable



Quanta Computer Inc.
PROJECT : ZK6

Size	Document Number	Rev
	ICH9M GPIO	1A

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ICH9M

IV@
EV@

Power consumption reference to Intel ICH9 Family EDS Rev 1.6

2~3.456v
3.6uA_G3

PER INTEL SUGGESTION:
CHANGE TO 100OHM & 1UF

5V
2mA

5V
S0:2mA
S3/4/5:1mA

1.5V
646mA

1.5V
47mA

VCC1_5_A
1.5V
1342mA

1.5V
11mA

1.05V , Powered by VCC1_05 in S0

3.3V
S0:19mA
S3/4/5:78mA

1.5V
23mA

1.5V
80mA

3.3V
1mA

1.05V
1634mA

1.5V
23mA

1.05V
50mA

1.05V
2mA

3.3V
308mA

1.5V / 3.3V
11mA

3.3V
S0:212mA
S3/4/5:53mA

1.5V / 3.3V
S0:11mA
S3/4/5:1mA

3.3V
S0:19mA
S3/4/5:73mA

VCCSUS1_05 power by VCC1_05 in S0 / VCCSUS3_3 in S3/S4/S5
VCCSUS1_5 power by VCC1_5_A in S0 / VCCSUS3_3 in S3/S4/S5

VCCCL1_05 power by VCC1_05_A in S0
VCCCL1_5 power by VCC1_5_A in S0

Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

Support INT HDMI HDA interface. These power only support 1.5V.Device must to meet.

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

If use SB MAC for LAN function. And support wake up need connect to relation power.

U29F — ICH9M REV 1.0

U29E — ICH9M REV 1.0

Quanta Computer Inc.		
PROJECT : ZK6		
Size	Document Number: ICH9 POWER	Rev 1A
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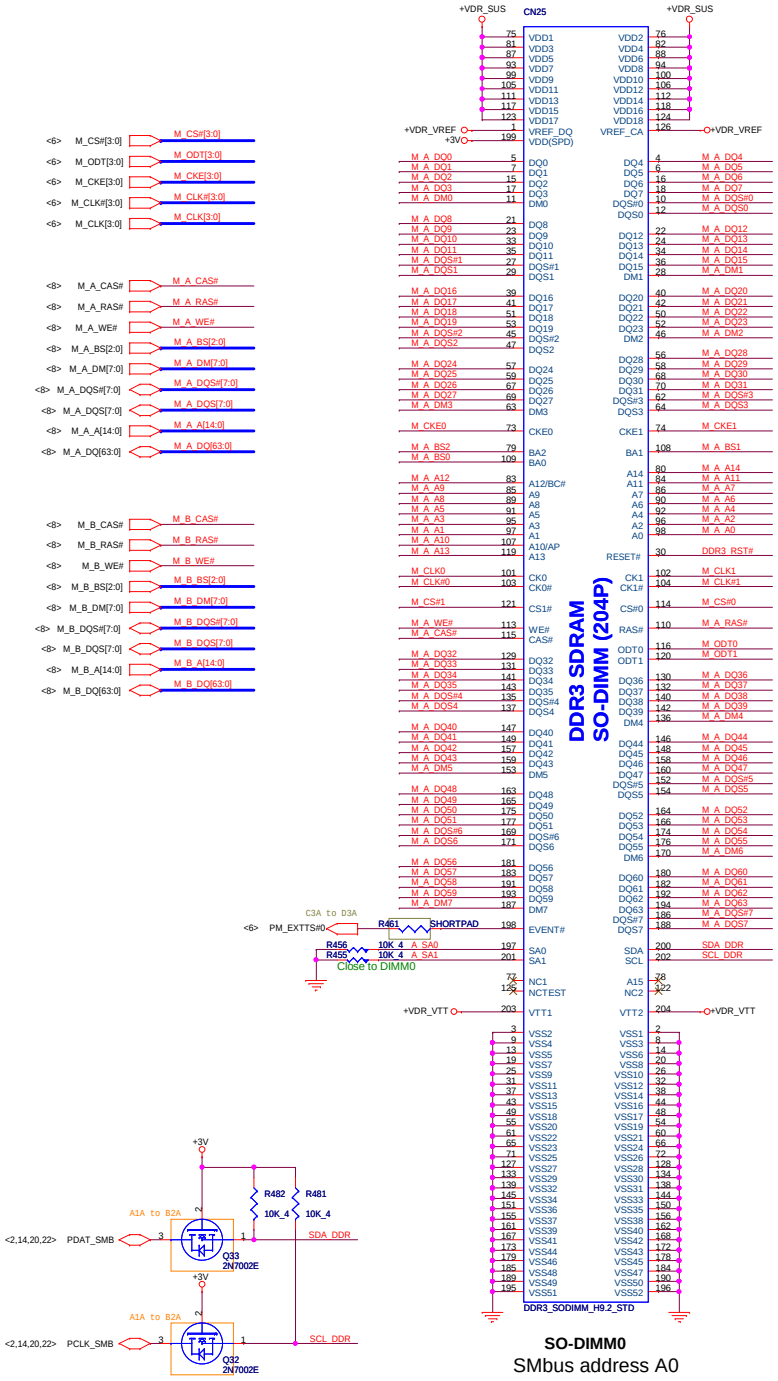
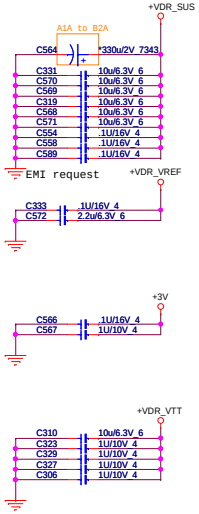
H=9.2mm / DGMK4000058



Decoupling capacitor

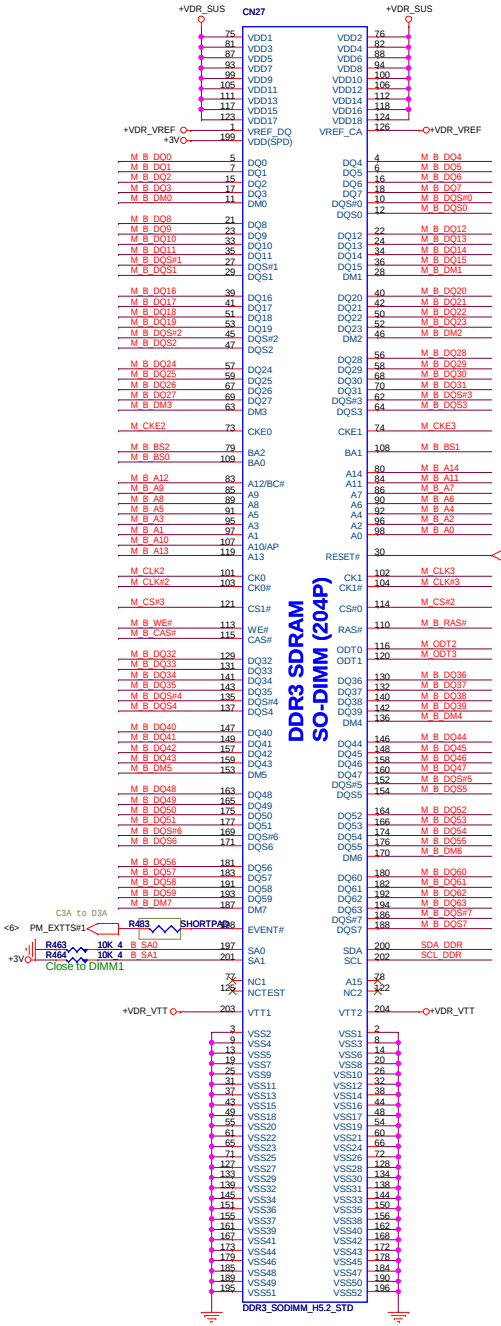
Close to SO-DIMM0



SO-DIMM0

SMbus address A0

H=5.2mm / DGMK4000059



Decoupling capacitor

Close to SO-DIMM1

SO-DIMM1

SMbus address A2

Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	DDRIII SO-DIMM	1A

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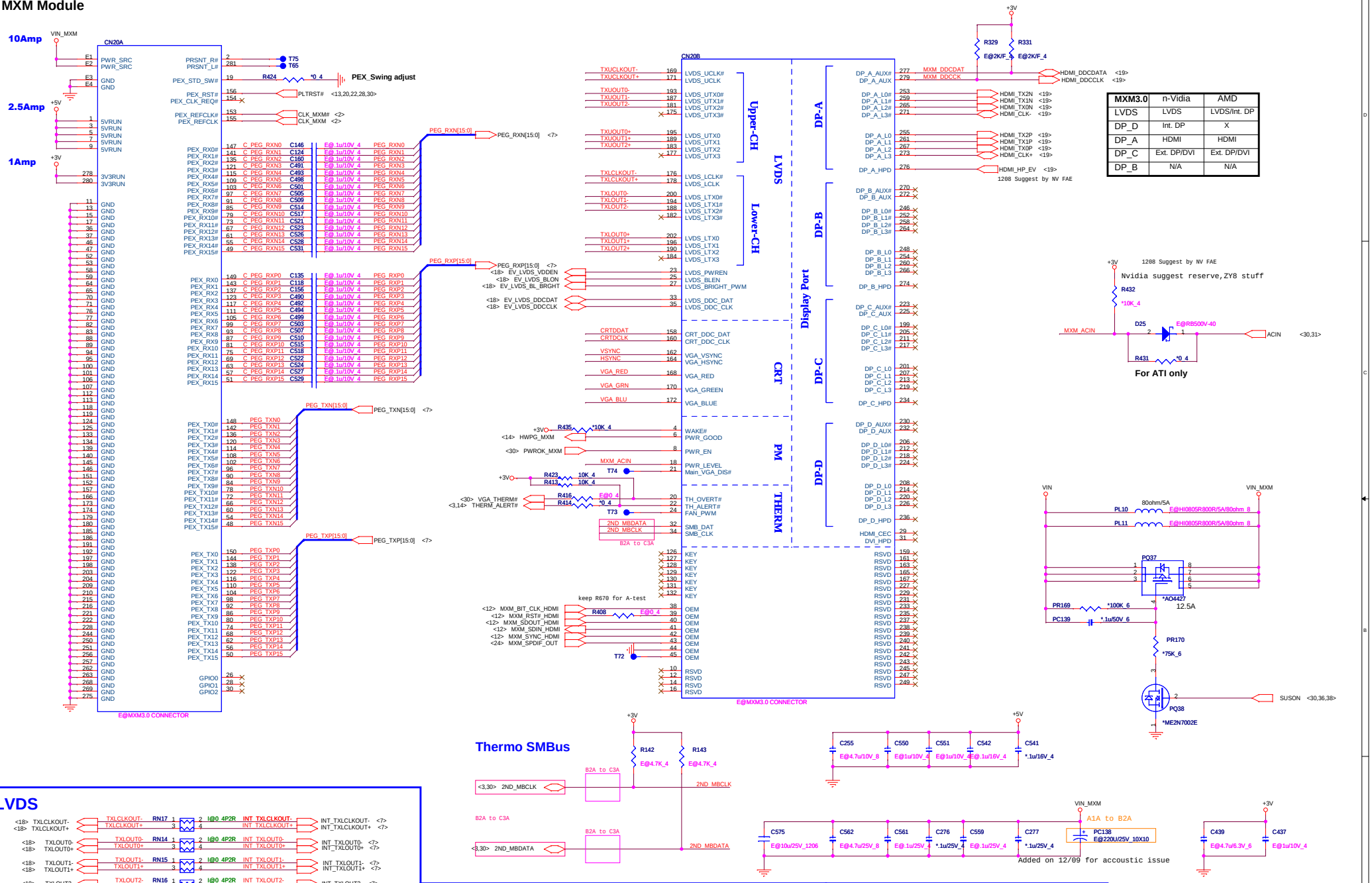
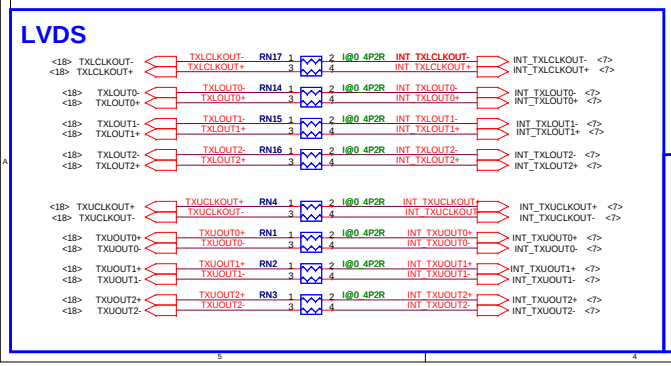
MXM Module

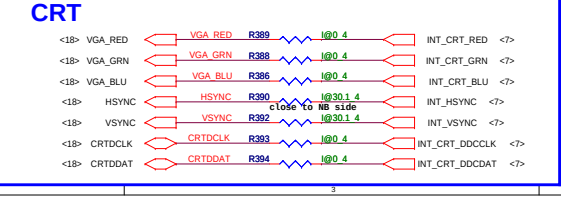


MXM3.0	n-Vidia	AMD
LVDS	LVDS	LVDS/Int. DP
DP_D	Int. DP	X
DP_A	HDMI	HDMI
DP_C	Ext. DP/DVI	Ext. DP/DVI
DP_B	N/A	N/A

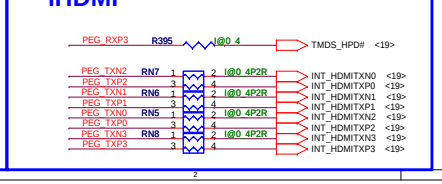
LVDS



CRT



iHDMI



Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	MXM3.0	1A

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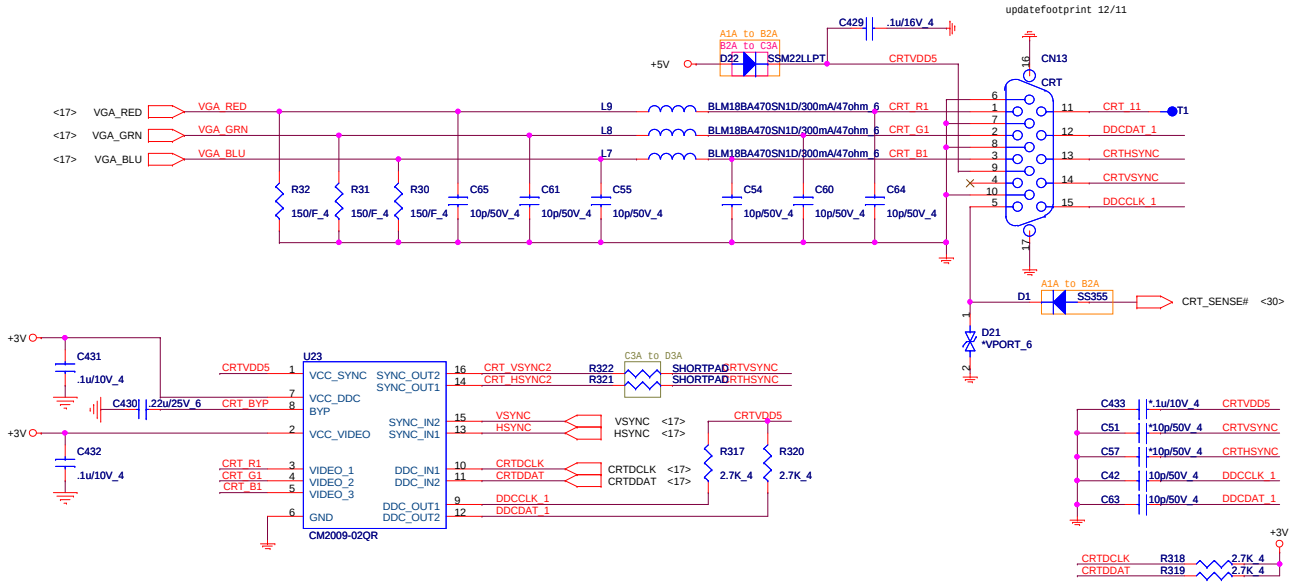
CRT

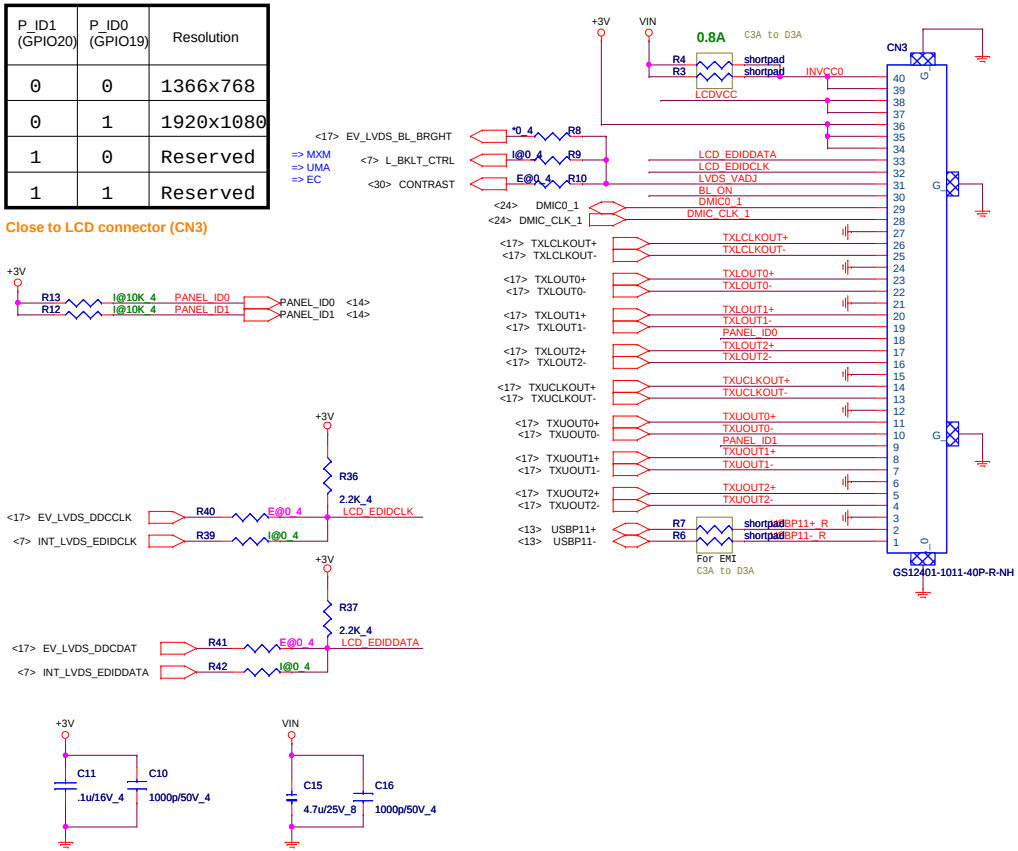
IV@
EV@



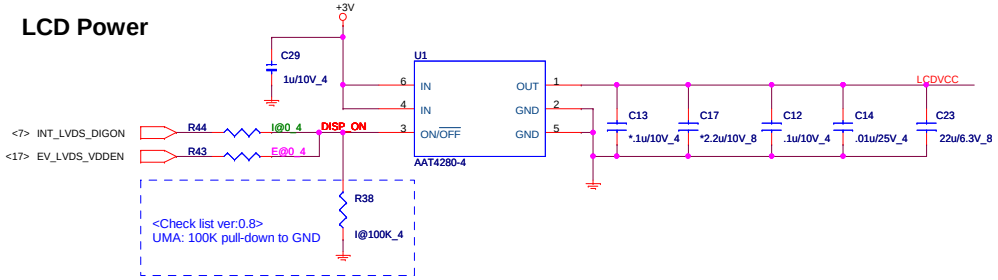
LVDS Panel ID (UMA only)

P_ID1 (GPIO20)	P_ID0 (GPIO19)	Resolution
0	0	1366x768
0	1	1920x1080
1	0	Reserved
1	1	Reserved

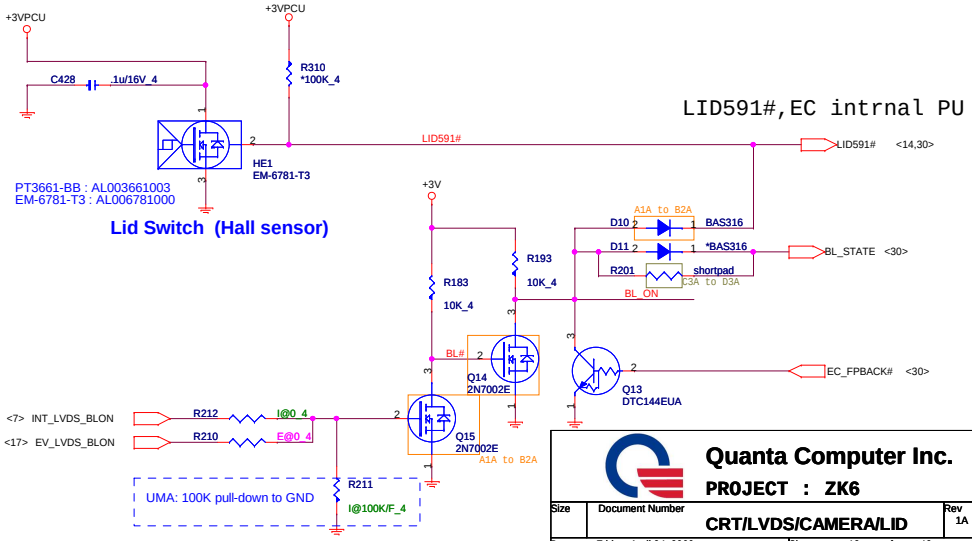
Close to LCD connector (CN3)



LCD Power



Backlight Control & LID



Quanta Computer Inc.
PROJECT : ZK6

Size	Document Number	Rev
	CRT/LVDS/CAMERA/LID	1A

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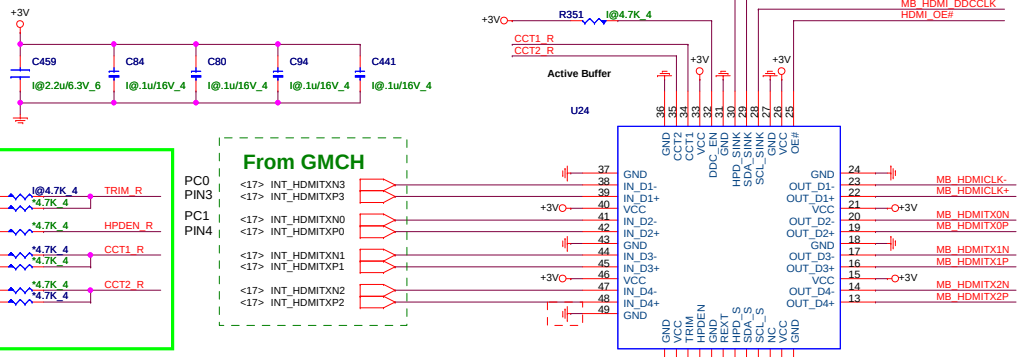
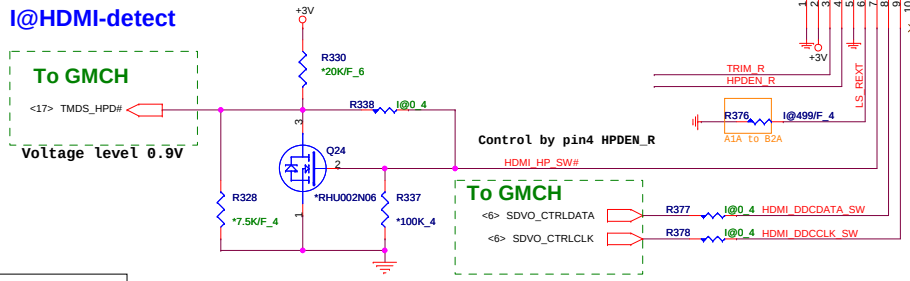
I@ HDMI LEVEL SHIFTER

CH7318C :: AL007318002
PS8101T :: AL008101001

IV@
EV@
SP@



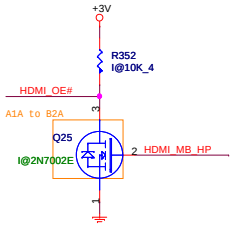
I@HDMI-detect



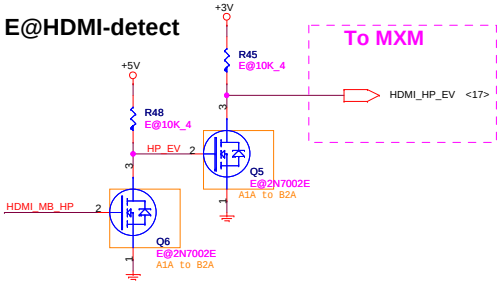
Voltage level 0.9V

Equalization Control		
PC1 PIN4	PC0 PIN3	EQ Control
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB

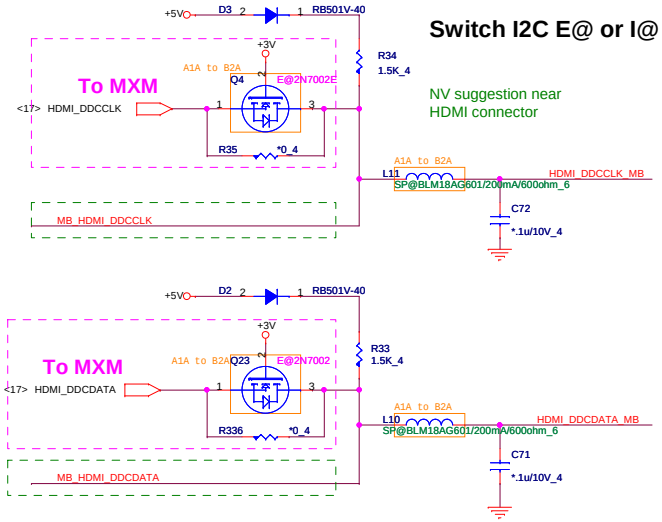
OE# control for power saving



E@HDMI-detect

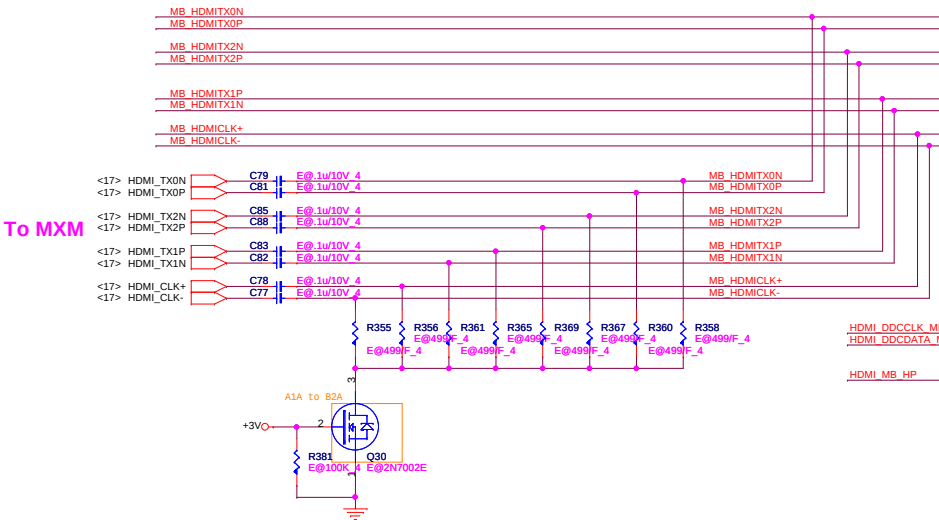


Switch I2C E@ or I@

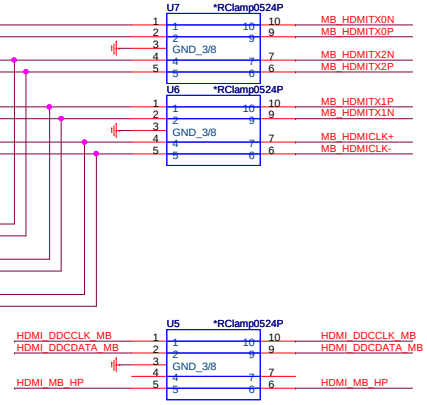


NV suggestion near HDMI connector

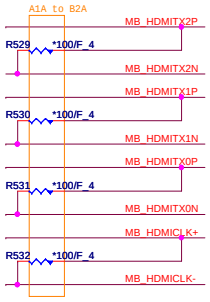
Switch E@ or I@

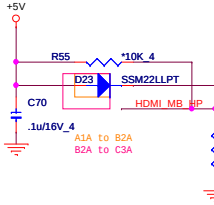


ESD Protect

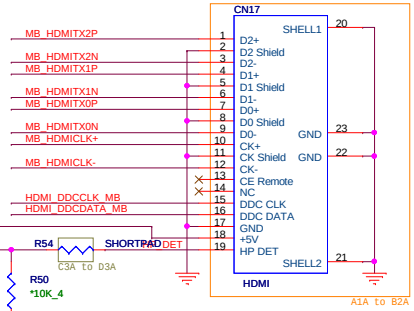


EMI



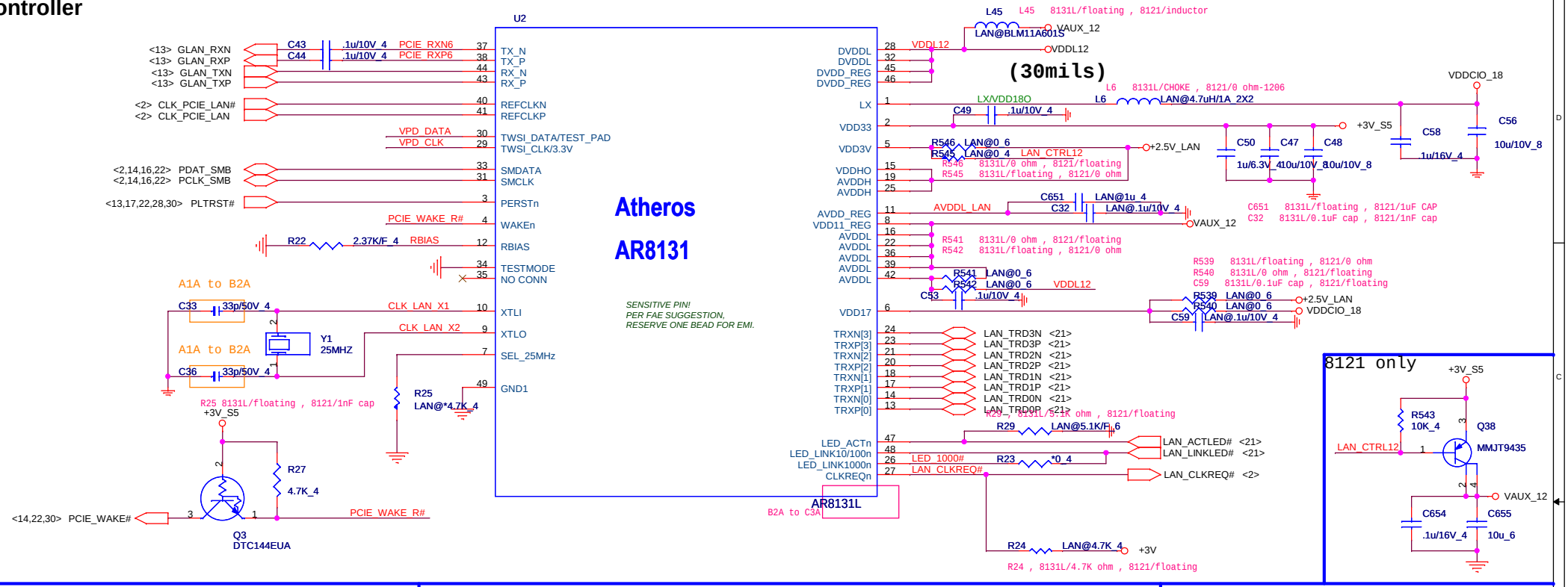


HDMI connector

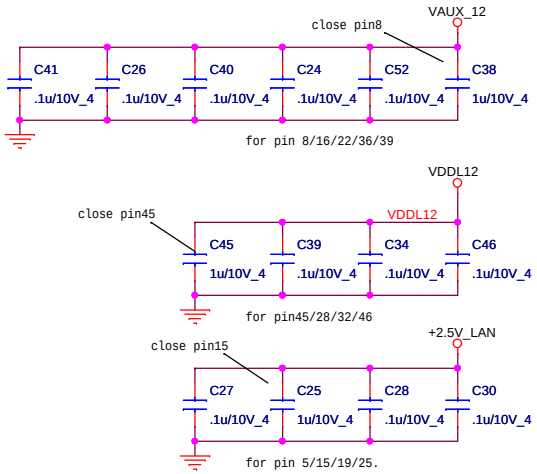


Quanta Computer Inc.		
PROJECT : ZK6		
Size	Document Number	Rev
	HDMI (CH7318C)	1A
Date: Friday, April 24, 2009	Sheet 19 of 42	

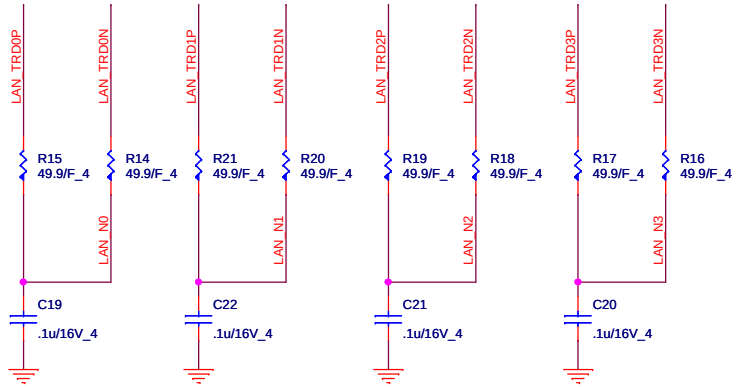
LAN Controller



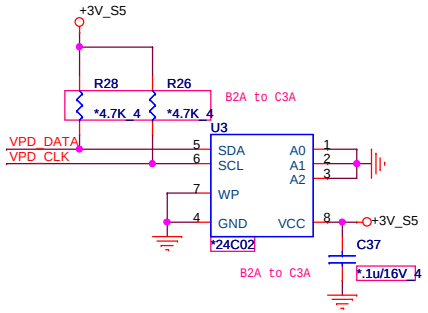
Decoupling CAP



PLACE NEAR IC SIDE



EEPROM



Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	AR8131 GLAN	1A

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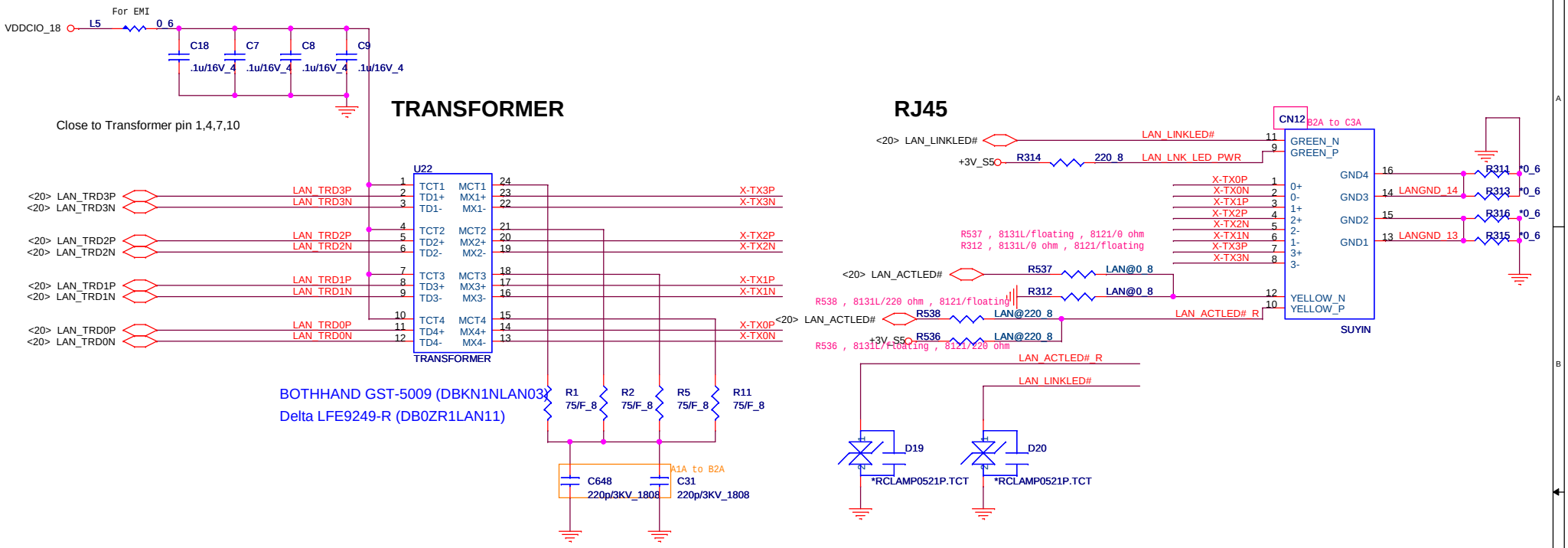
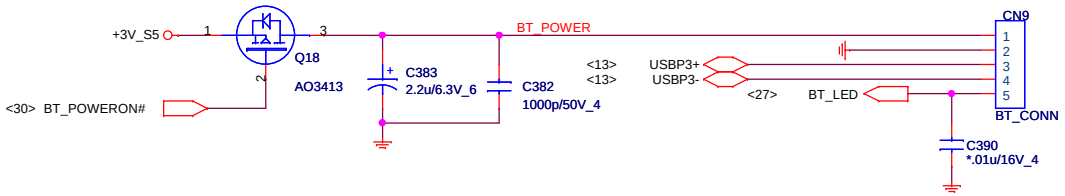


BLUETOOTH CONNECTOR

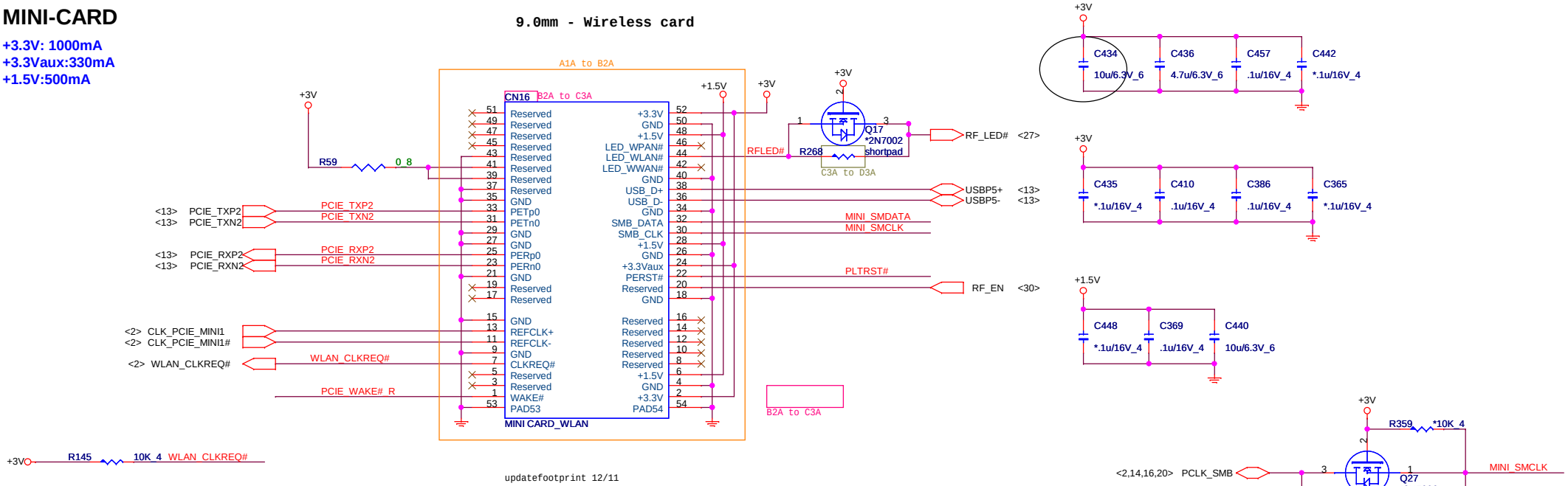


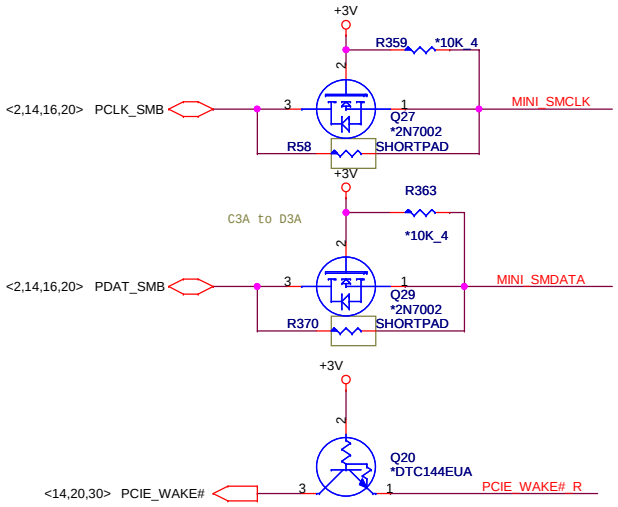
Quanta Computer Inc.		
PROJECT : ZK6		
Size	Document Number	Rev
	LAN Transformer and RJ45/BT	1A
Date: Friday, April 24, 2009	Sheet 21 of 42	

MINI-CARD

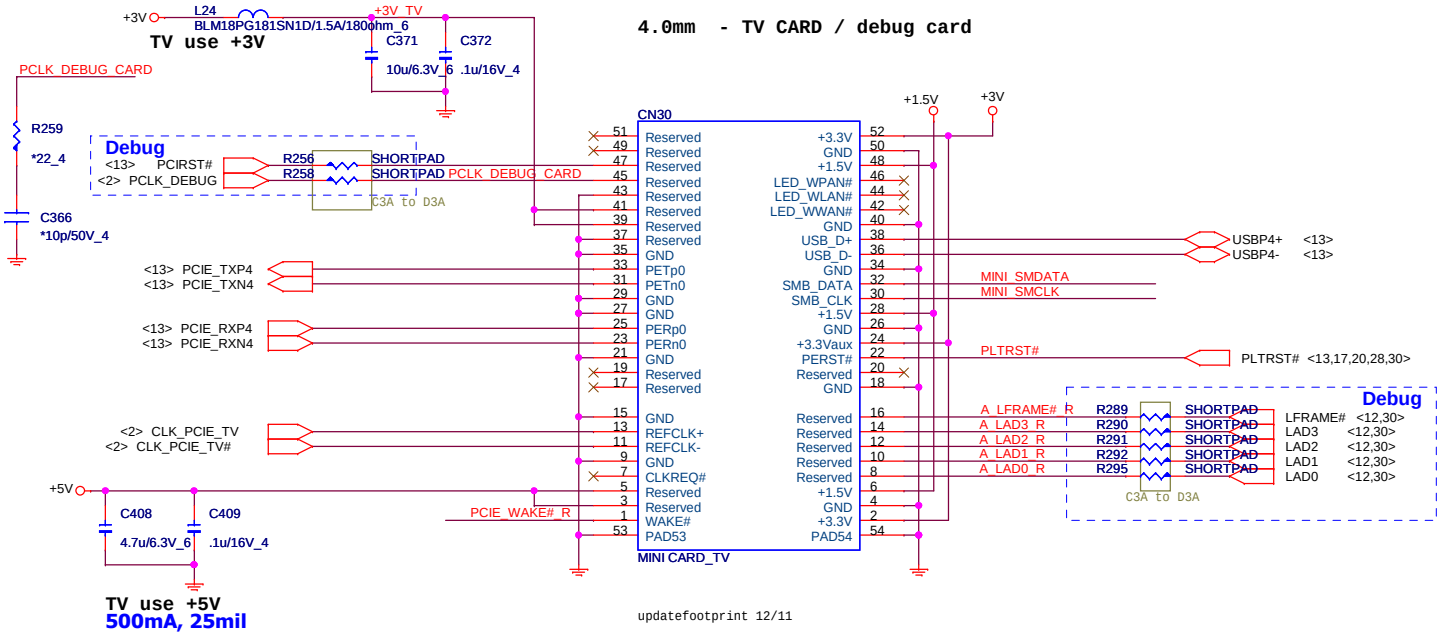
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

9.0mm - Wireless card





4.0mm - TV CARD / debug card



Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	MINI PCI-E card/TV	1A

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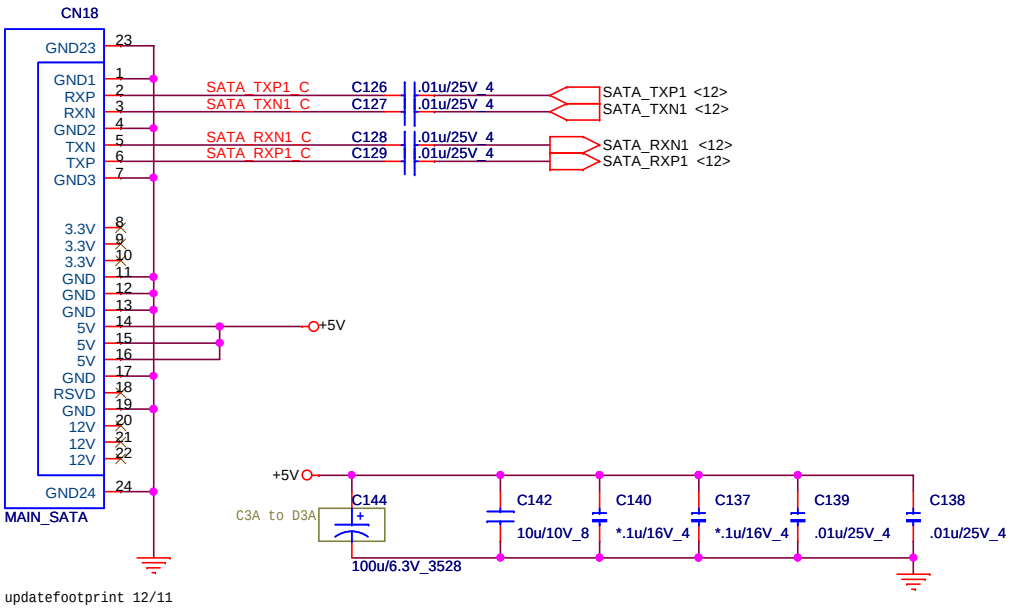
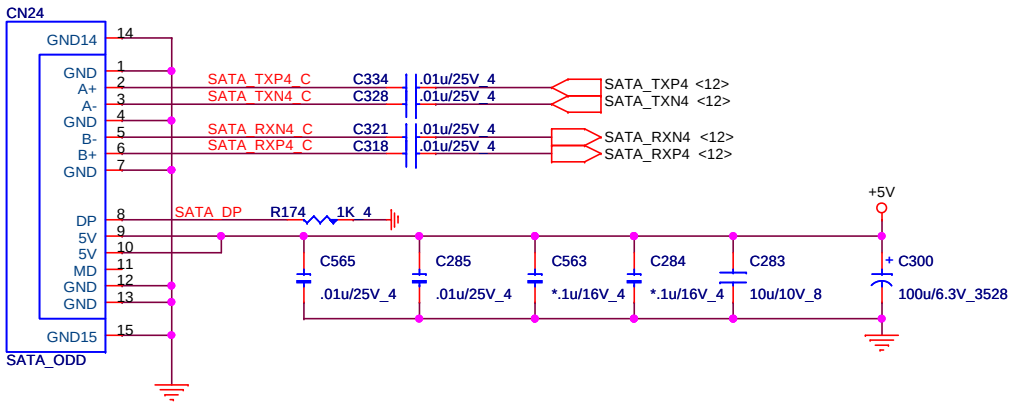
MAIN SATA HDD



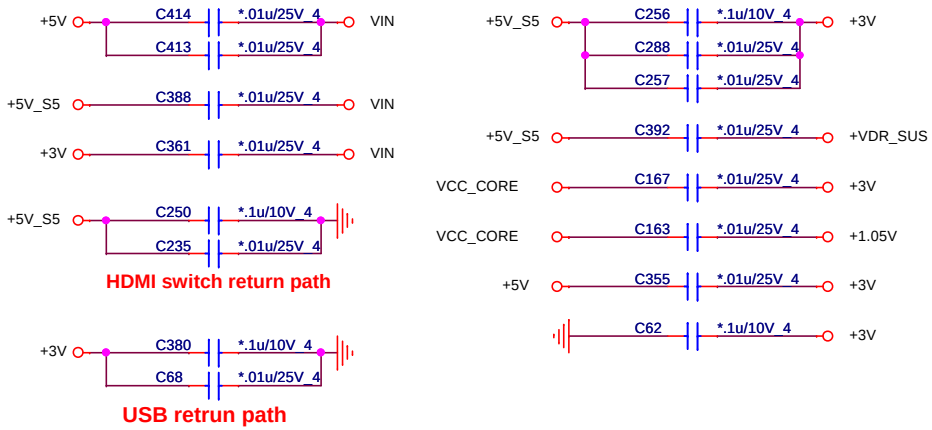
updatefootprint 12/11

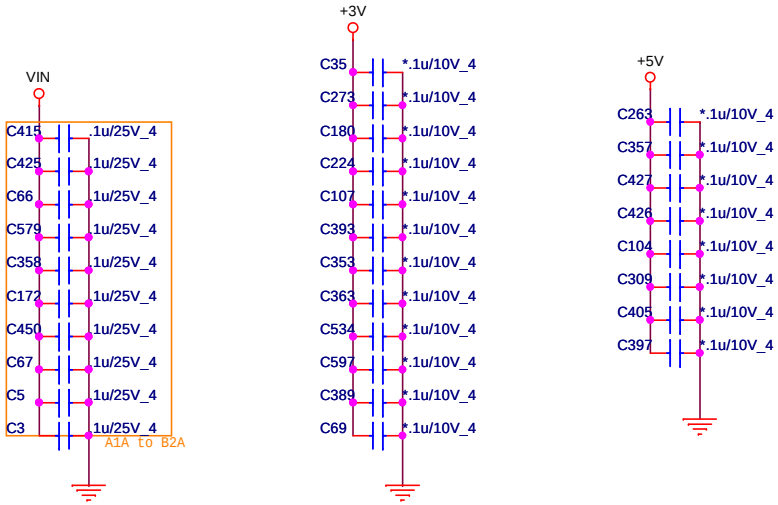
ODD (SATA)



updatefootprint 12/11

EE RETURN-PATH CAPACITORS





Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	1A
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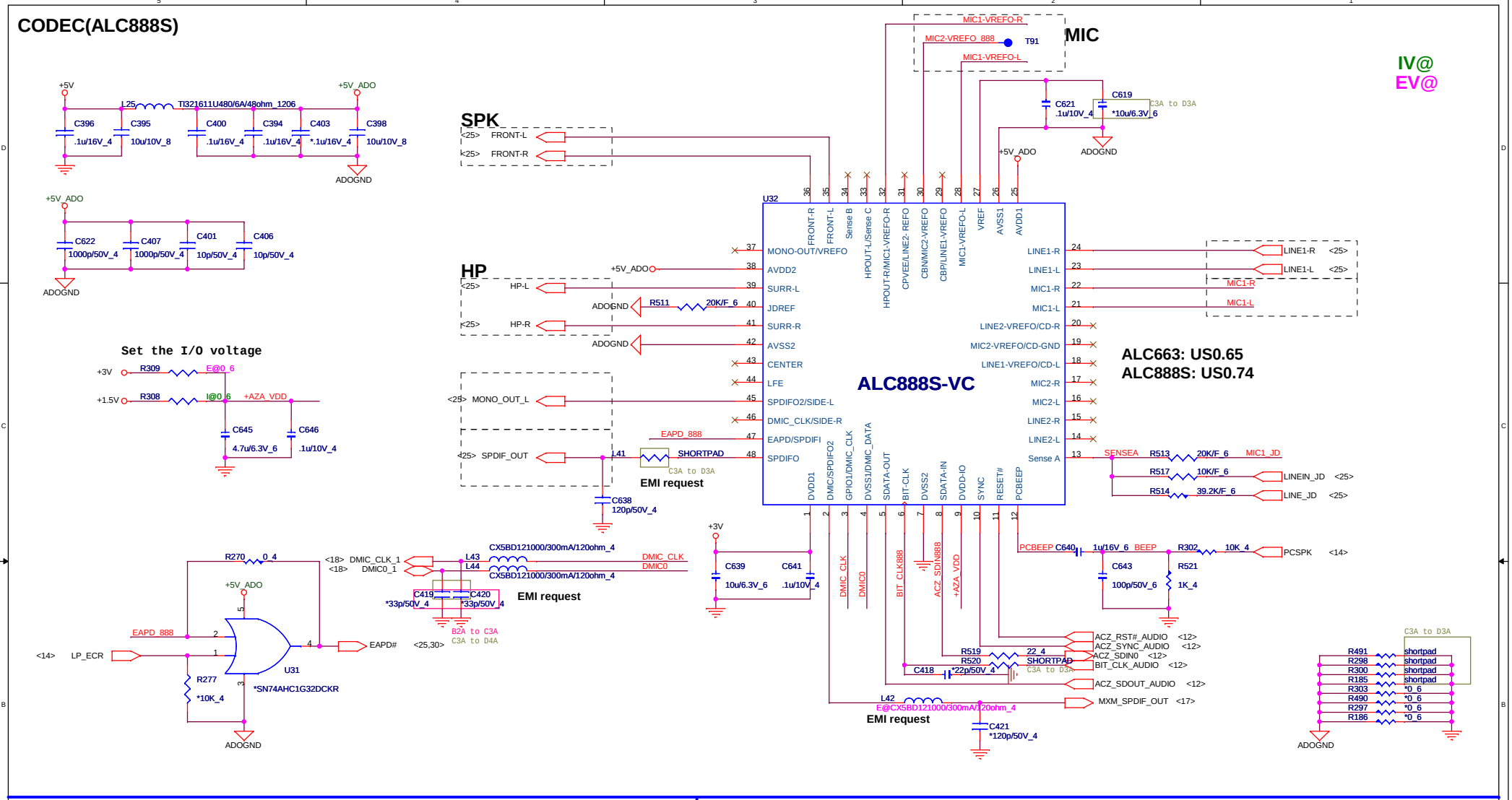
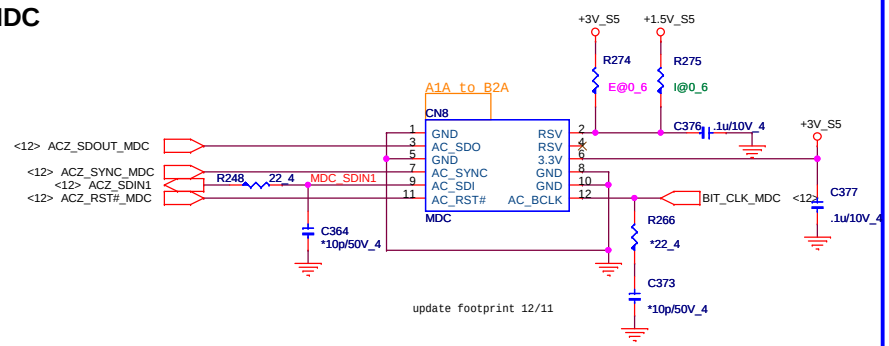
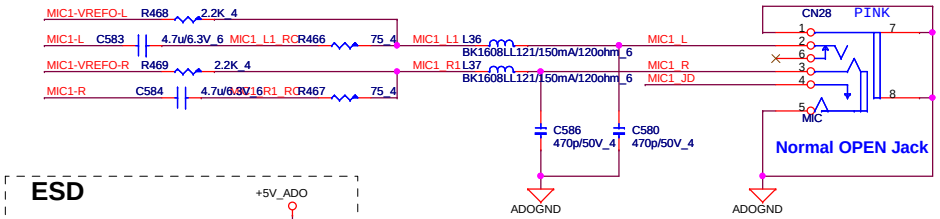
CODEC(ALC888S)



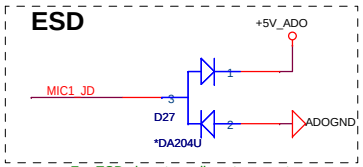
MDC



MIC



ESD



For ESD close to audio out connecter

CODEC & MDC

Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	REALTEK ALC663&888/MDC	1A

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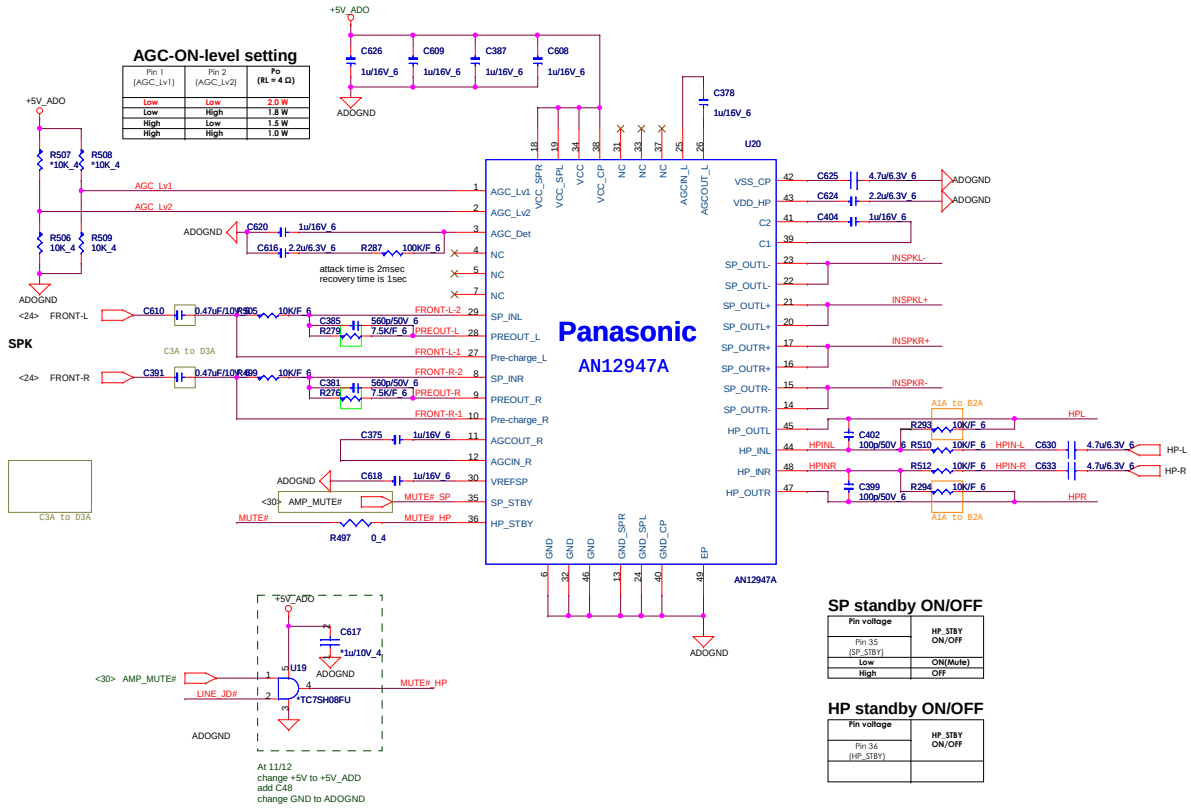
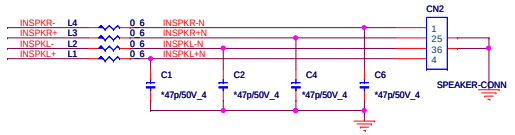
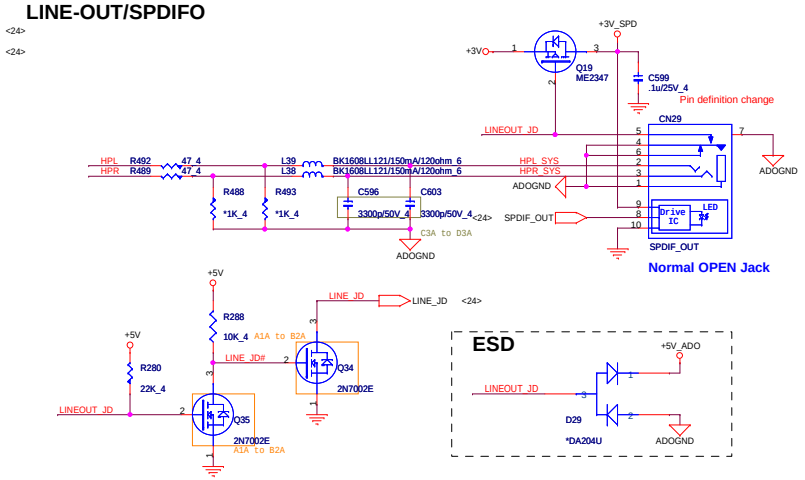
SPEAKER/HP AMP.



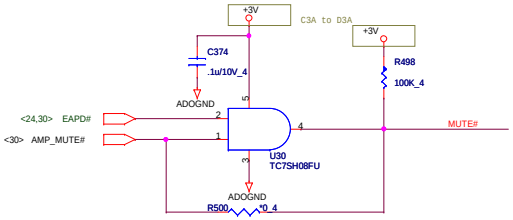
SPEAKER



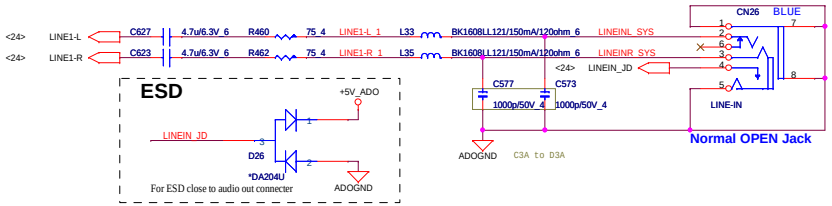
LINE-OUT/SPDIFO



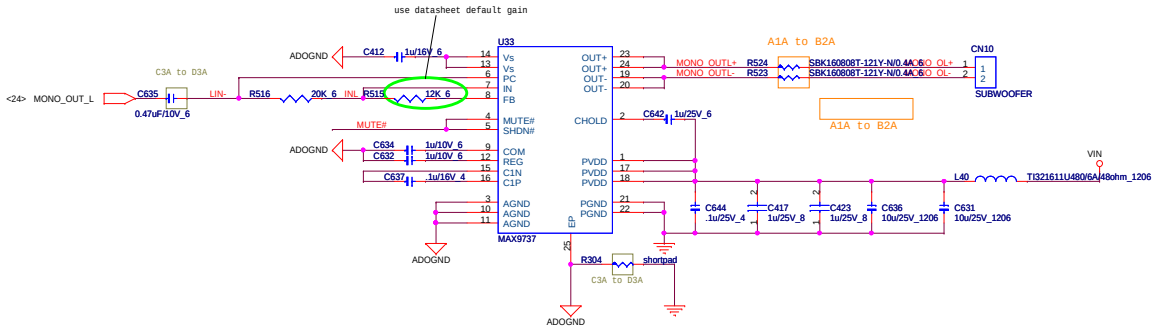
MUTE



LINE IN



SUBWOOFER



AMP& PHONE JACK & SUBWOOFER

Quanta Computer Inc.
PROJECT : ZK6

Size	Document Number	Rev
	AMP /AUDIO JACK CONN	1A

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Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	CARD READER RTS5159	1A

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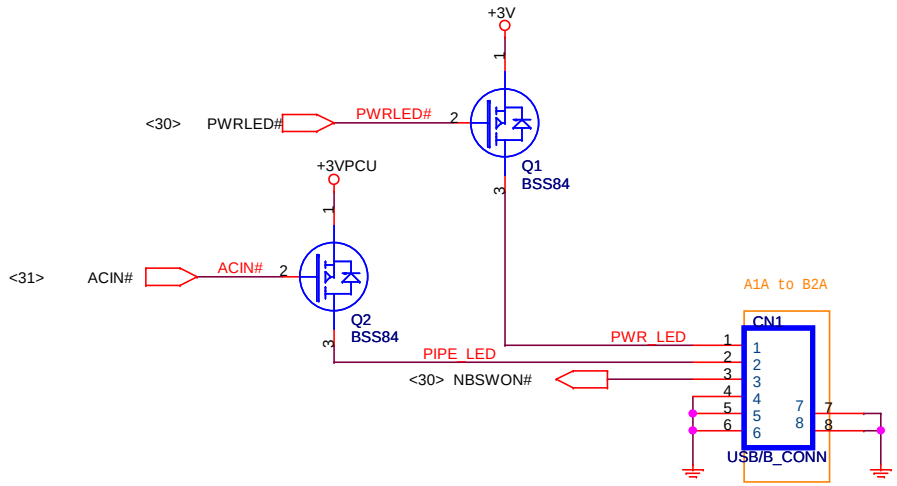
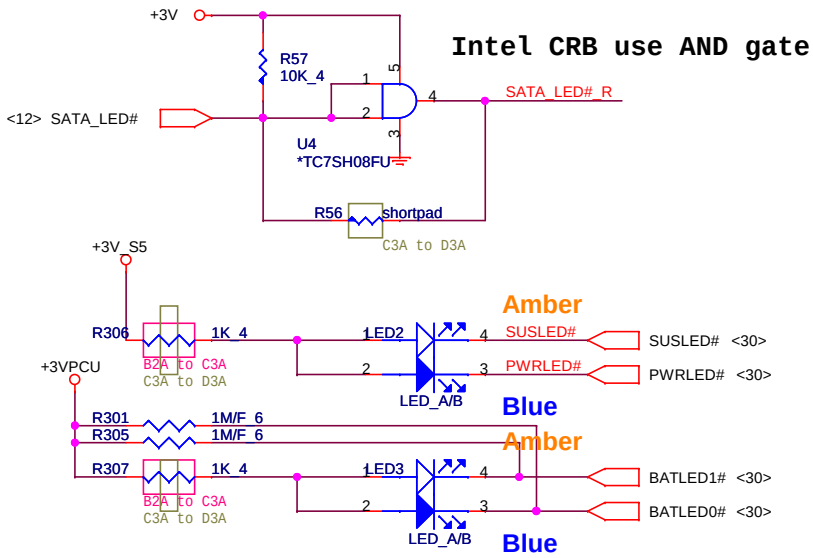
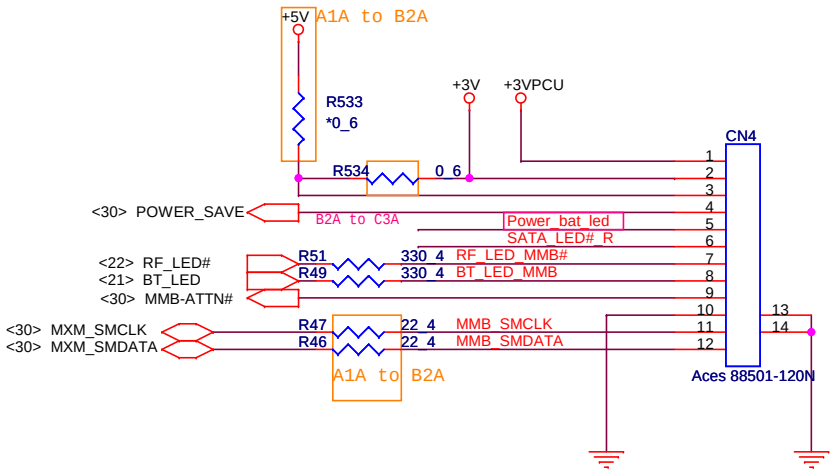
POWER BOARD



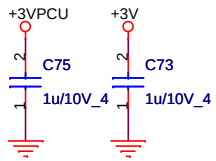
LED

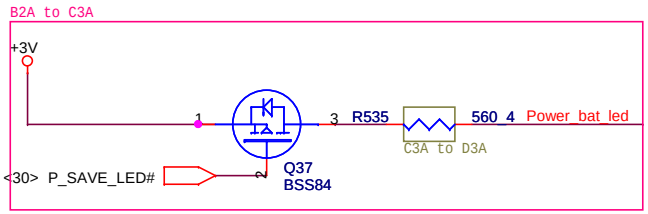


MMB



Close to MMB connector





Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	POWER/MMB/LAUNCH/LED	1A

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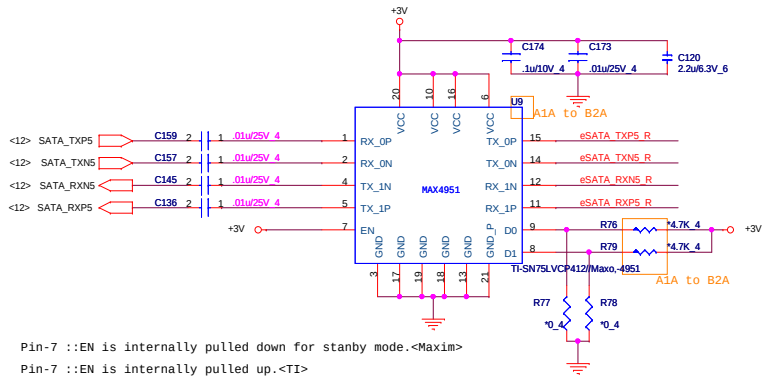
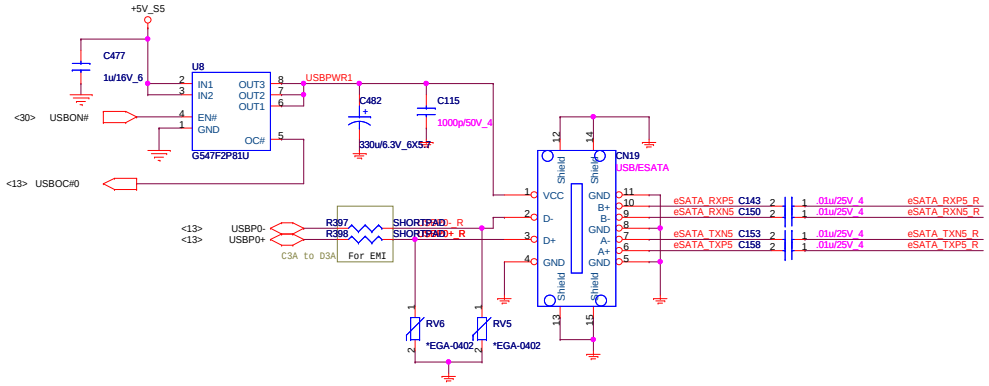
ESATA





Pin-7 ::EN is internally pulled down for stanby mode.<Maxim>

Pin-7 ::EN is internally pulled up.<TI>

Pin-8 ::BB is internally pulled down.<TI/MAXIM>

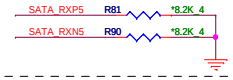
Pin-9 ::BA is internally pulled down.<TI/MAXIM>

EN	BA/D0	BB/D1	CH-0/A	CH-1/B
0	X	X	Standby	Standby
1	0	0	0dB	0dB
1	1	0	Pre-emphasis (5dB)	0dB
1	0	1	0dB	Pre-emphasis (5dB)
1	1	1	Pre-emphasis (5dB)	Pre-emphasis (5dB)

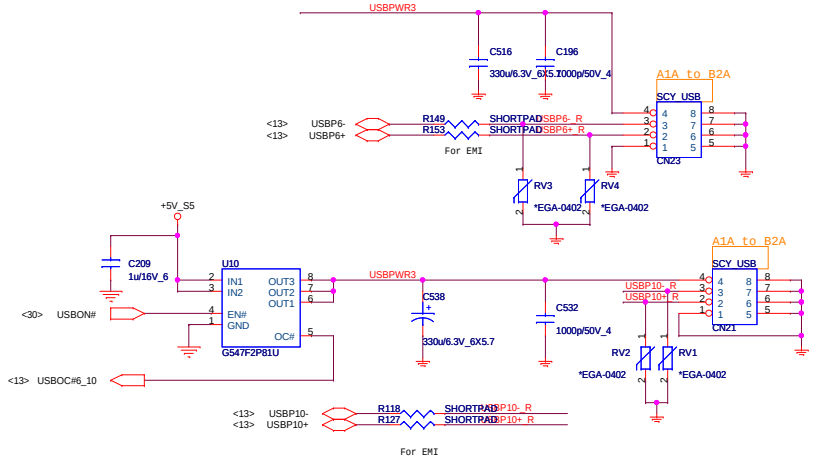
X=don't care

DG2.1 4.2.4 Terminating Unused SATA Interface

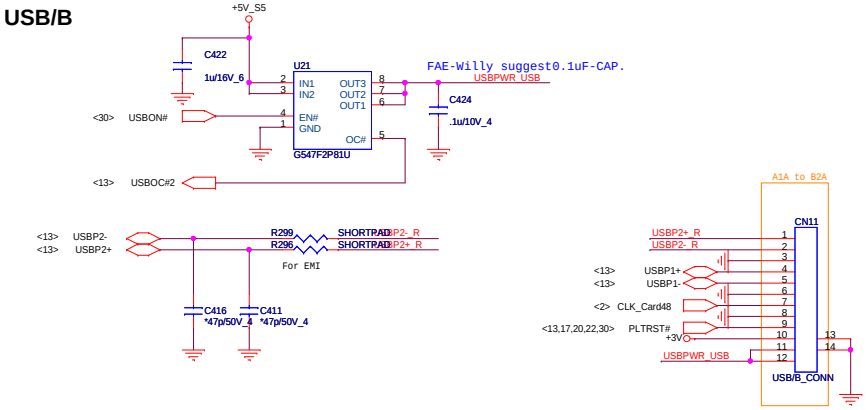
SATA[1:0]RXp/n, SATA[5:4]RXp/n connect to GND while SATA not be implemented



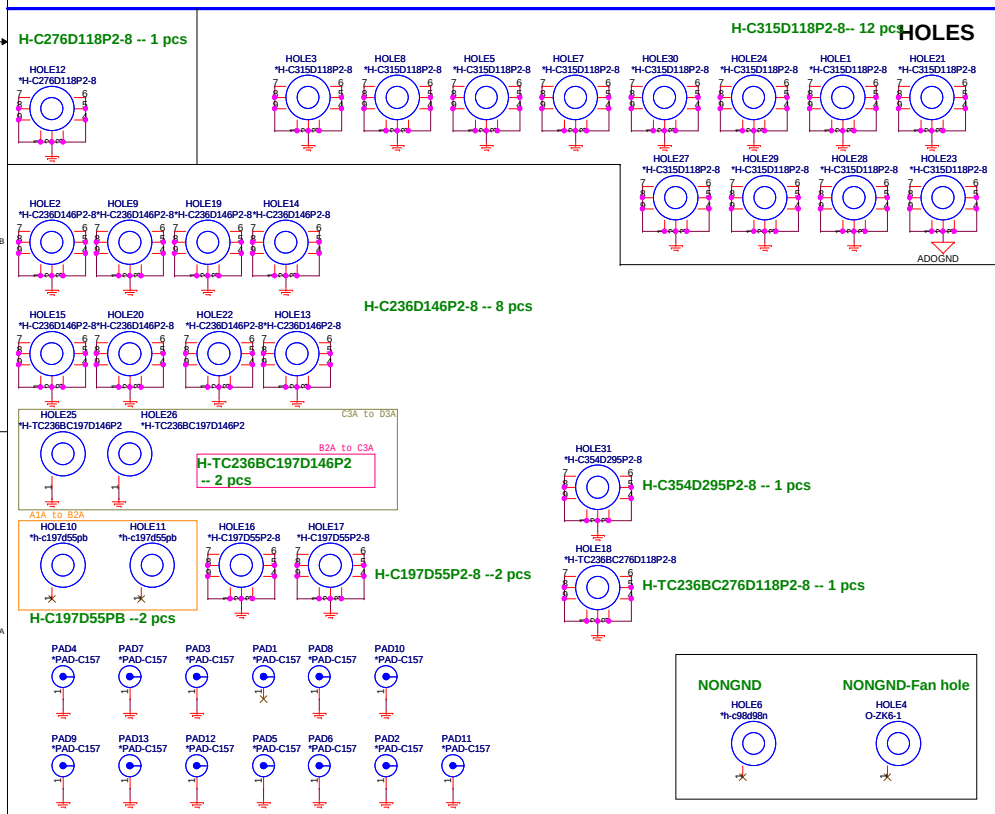
USB PORT



USB/B



HOLES



Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	USB	1A

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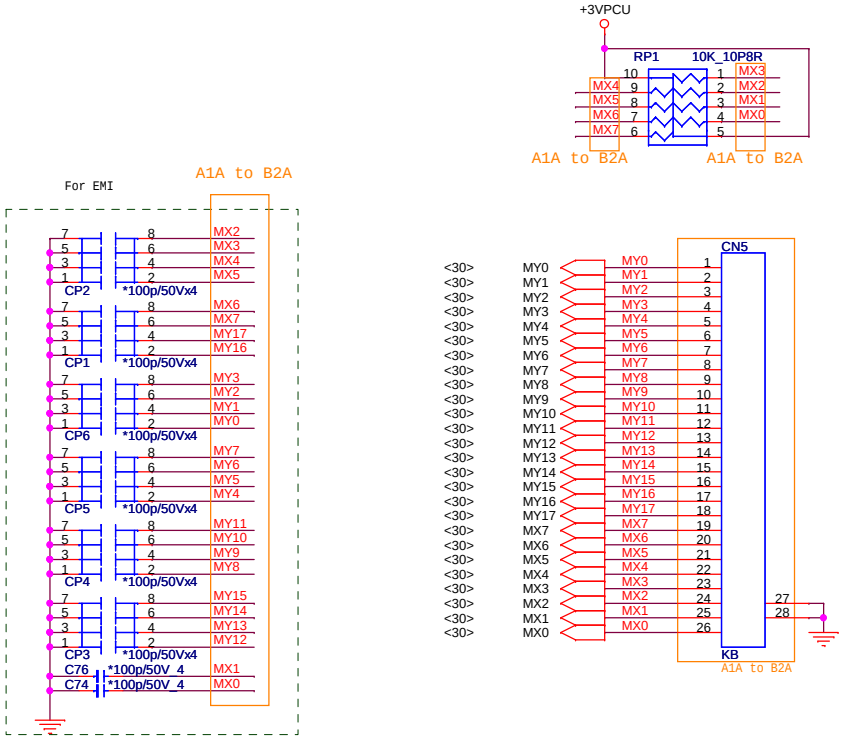
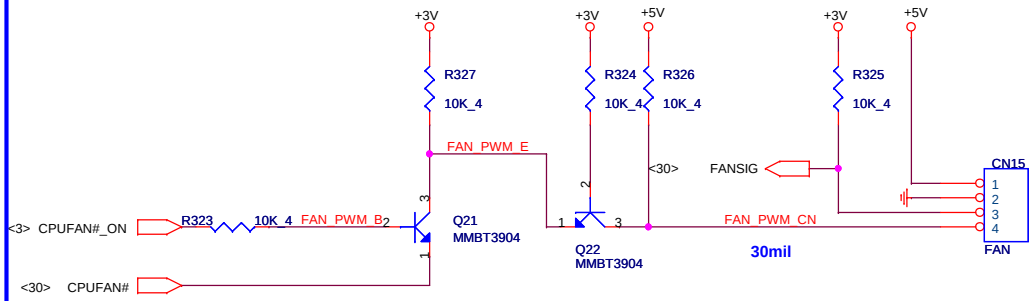
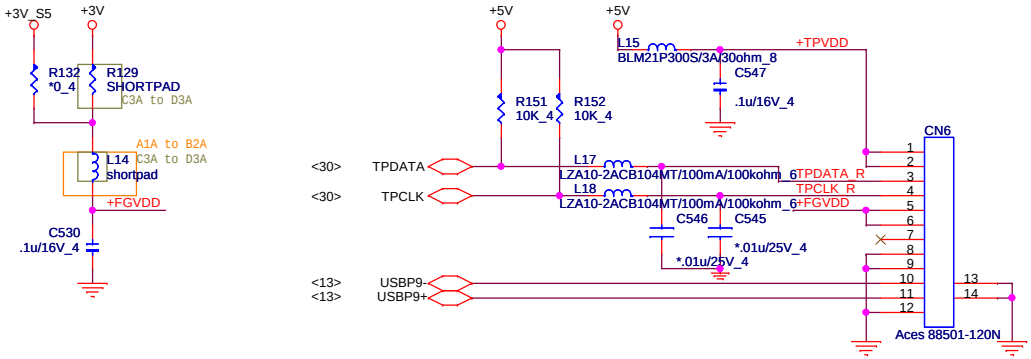
K/B



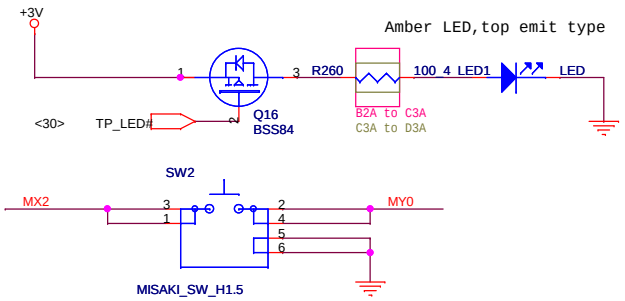
CPU FAN



TOUCHPAD & Finger-Printer CONN.



TP LOCK Button



Quanta Computer Inc.		
PROJECT : ZK6		
Size	Document Number	Rev
	KB/FAN/TP+FP	1A
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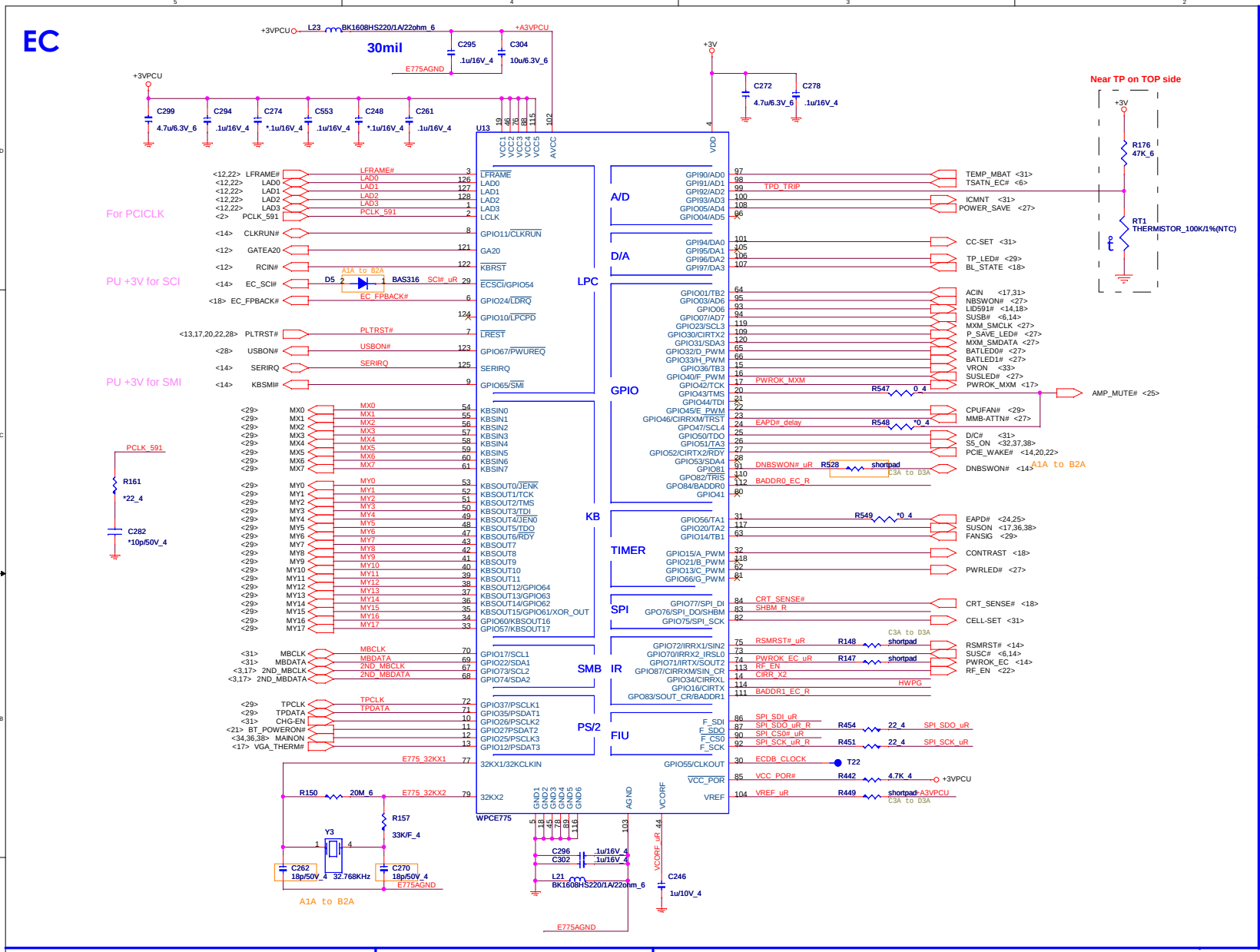
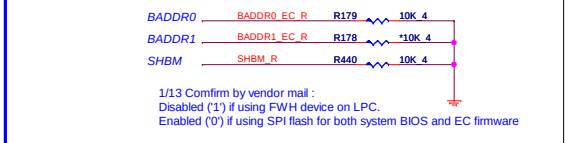
EC



I/O ADDRESS SETTING

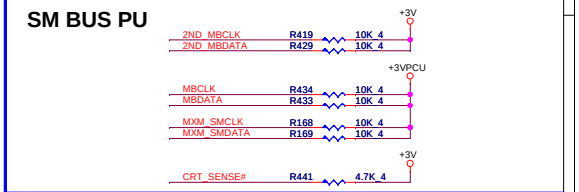
	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

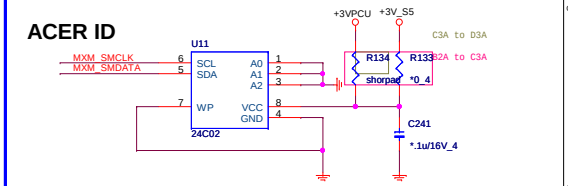


1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

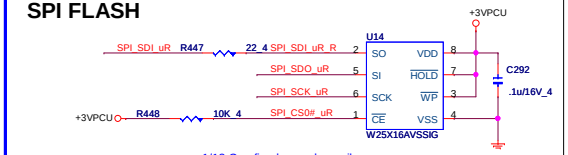
SM BUS PU



ACER ID

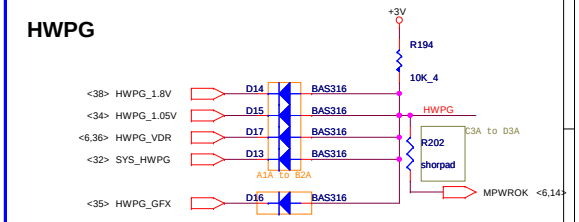


SPI FLASH

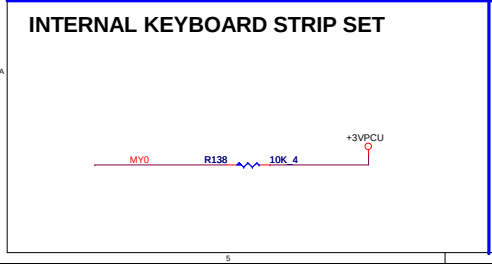


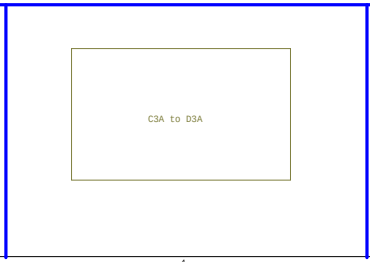
1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

HWPG

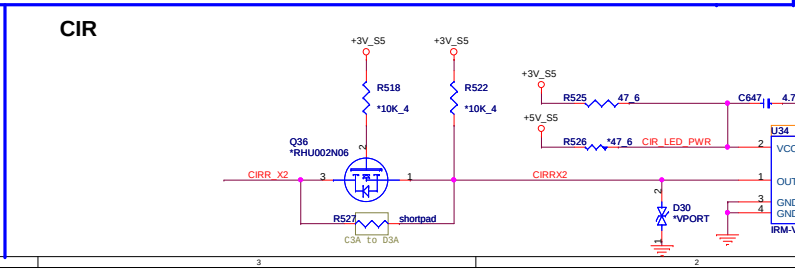


INTERNAL KEYBOARD STRIP SET





CIR

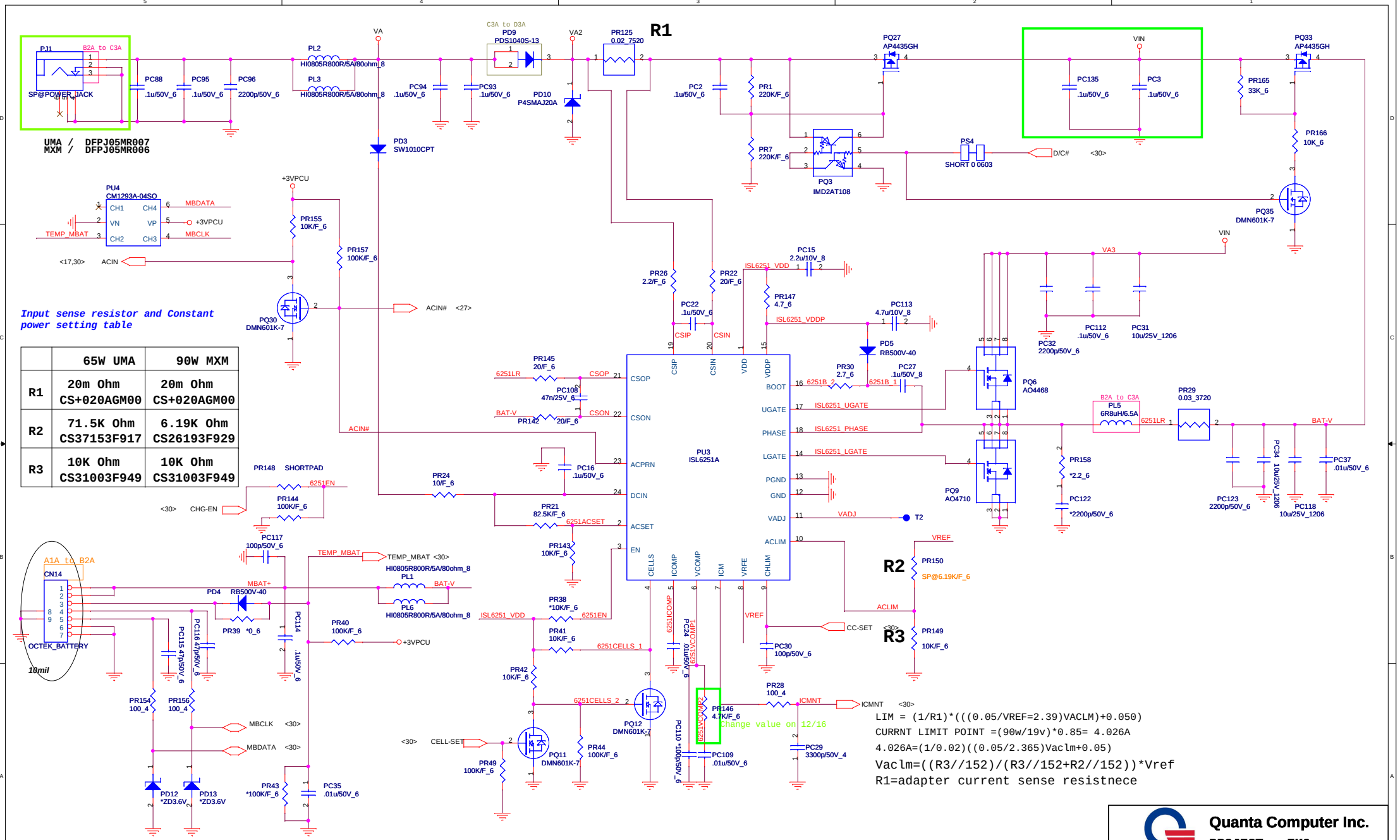


Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	WPCE775C_0DG & FLASH	1A

Date: Friday, April 24, 2009 Sheet 30 of 42



Input sense resistor and Constant power setting table

	65W UMA	90W MXM
R1	20m Ohm CS+020AGM00	20m Ohm CS+020AGM00
R2	71.5K Ohm CS37153F917	6.19K Ohm CS26193F929
R3	10K Ohm CS31003F949	10K Ohm CS31003F949

LIM = (1/R1)*(((0.05/VREF=2.39)VACLM)+0.050)
CURRNT LIMIT POINT =(90w/19v)*0.85= 4.026A
4.026A=(1/0.02)((0.05/2.365)Vaclm+0.05)
Vaclm=((R3//152)/(R3//152+R2//152))*Vref
R1=adapter current sense resistnece

CELL-SET = Hi ----> Cells = VDD ---->4S
CELL-SET = Low ----> Cells = GND ---->3S

Quanta Computer Inc.
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Size	Document Number	Rev
	CHARGER (ISL6251A)	1A

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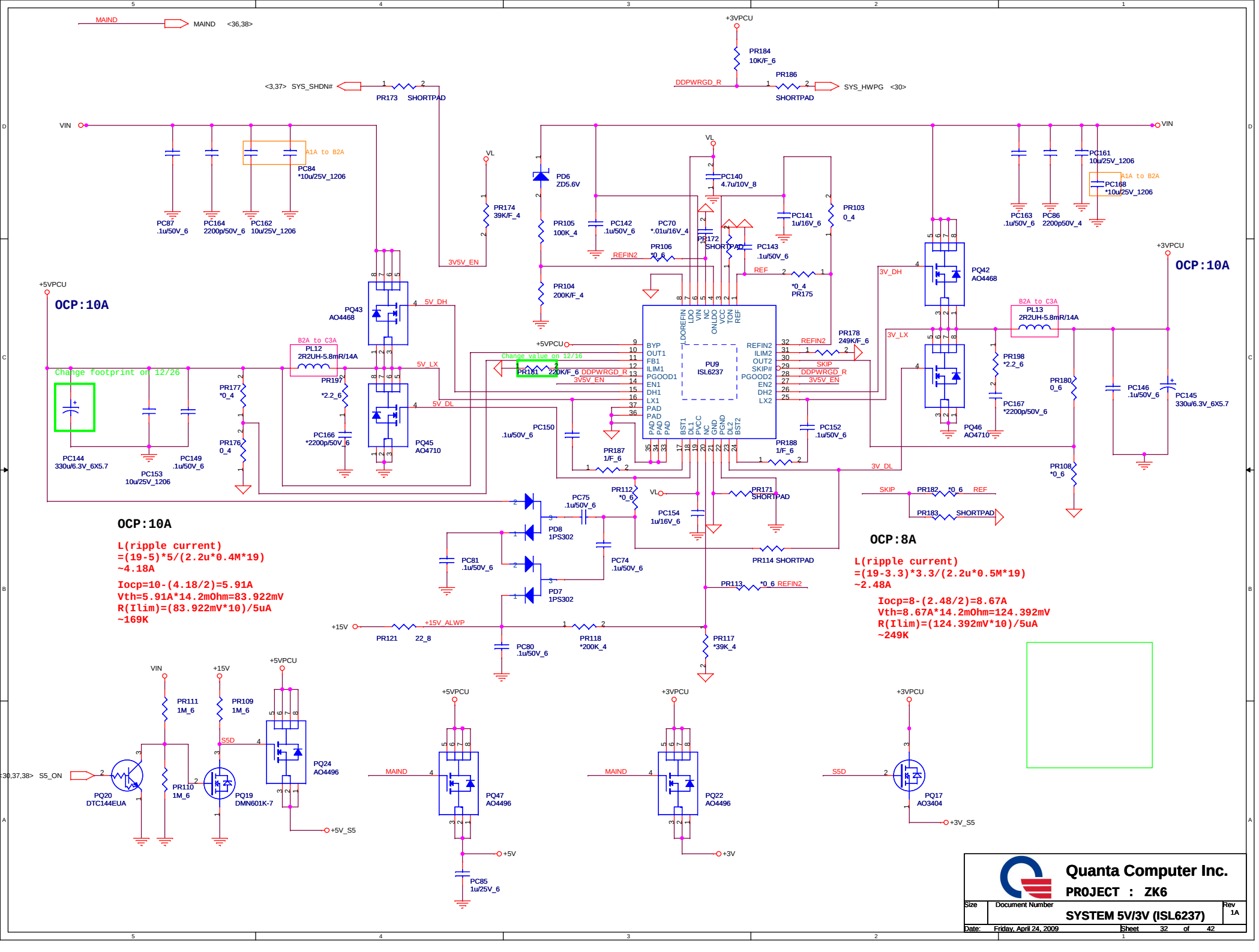
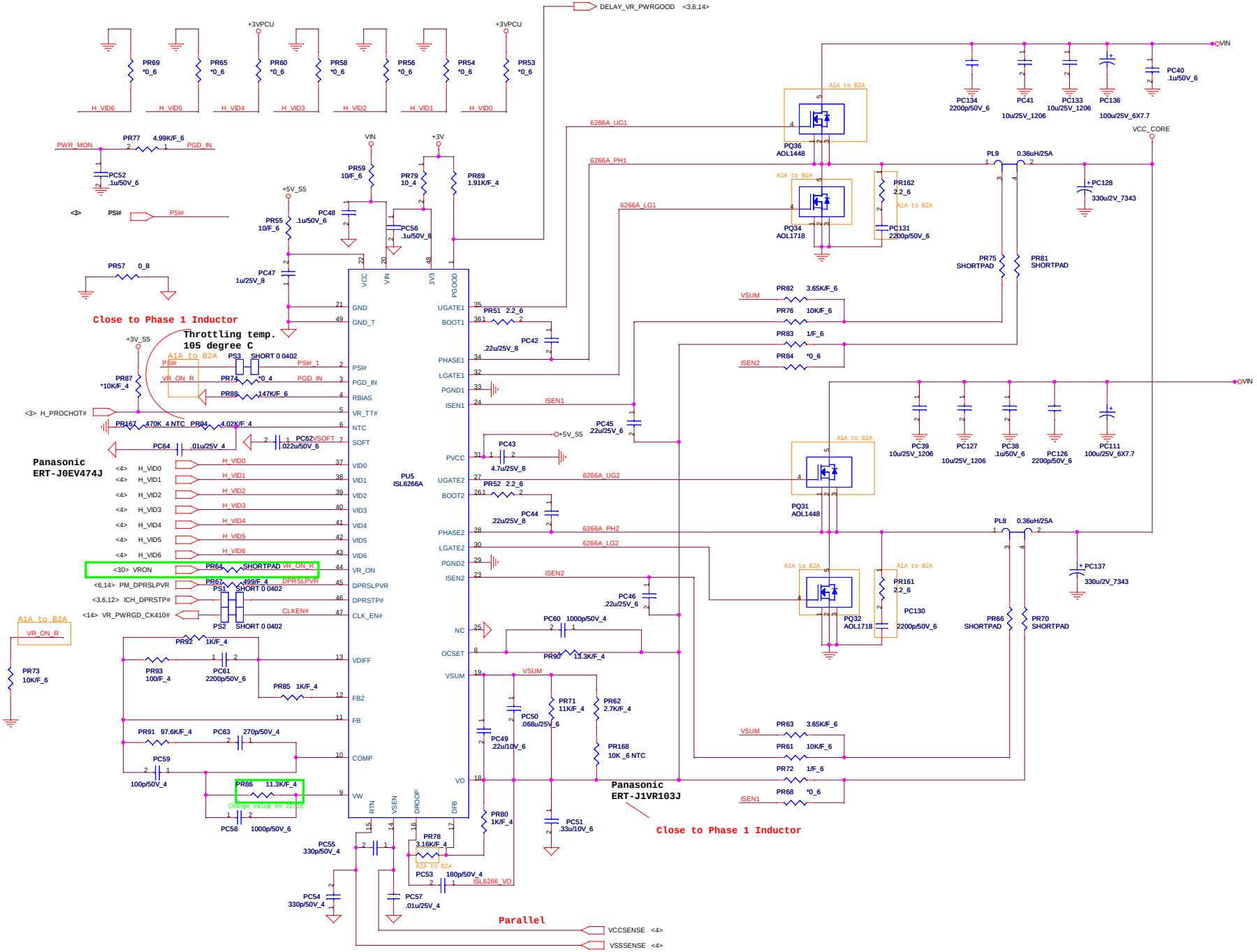

MAIND
MAIND <36,38>
+3VPCU
PR184
10K/F_6
PR186
SHORTPAD
DDPWRGD_R
SYS_HWPG <30>
<3,37> SYS_SHDN#
PR173 SHORTPAD
VIN
A1A to B2A
PC84
*10u/25V_1206
PC87
.1u/50V_6
PC164
2200p/50V_6
PC162
10u/25V_1206
VL
PR174
39K/F_4
3V5V_EN
PD6
ZD5.6V
PR105
100K_4
PC142
.1u/50V_6
PC70
*.01u/16V_4
PR106
*0_6
REFIN2
PR172
SHORTPAD
PC140
4.7u/10V_8
PC143
.1u/50V_6
PC141
1u/16V_6
PR103
0_4
REF
*0_4
PR175
PR104
200K/F_4
PC161
10u/25V_1206
PC168
*10u/25V_1206
PC163
.1u/50V_6
PC86
2200p50V_4
+3VPCU
OCP:10A
+5VPCU
OCP:10A
PQ43
AO4468
5V_DH
B2A to C3A
PL12
2R2UH-5.8mR/14A
5V_LX
Change footprint on 12/26
PR177
*0_4
PR197
*2.2_6
PR176
0_4
PC166
*2200p/50V_6
PQ45
AO4710
5V_DL
PC144
330u/6.3V_6X5.7
PC153
10u/25V_1206
PC149
.1u/50V_6
+5VPCU
Change value on 12/16
PR181 220K/F_6 DDPWRGD_R
3V5V_EN
PU9
ISL6237
LDOREFIN
LDO
VIN
NC
ONLDO
VCC
TON
REF
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
BST1
DL1
PVCC
GND
DL2
BST2
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
PC150
.1u/50V_6
PR187
1/F_6
PR188
1/F_6
PC152
.1u/50V_6
PR178
249K/F_6
SKIP
3V_DH
3V_LX
3V_DL
PQ42
AO4468
PQ46
AO4710
PR198
*2.2_6
PC167
*2200p/50V_6
PR180
0_6
PR108
*0_6
PC146
.1u/50V_6
PC145
330u/6.3V_6X5.7
PR112
*0_6
PC75
.1u/50V_6
PC154
1u/16V_6
PR171
SHORTPAD
PR182 *0_6 REF
PR183 SHORTPAD
PD8
1PS302
PC81
.1u/50V_6
PC74
.1u/50V_6
PR114 SHORTPAD
PR113 *0_6 REFIN2
PD7
1PS302
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=8.67A
Vth=8.67A*14.2mOhm=124.392mV
R(Ilim)=(124.392mV*10)/5uA
~249K
OCP:10A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A
Iocp=10-(4.18/2)=5.91A
Vth=5.91A*14.2mOhm=83.922mV
R(Ilim)=(83.922mV*10)/5uA
~169K
+15V
PR121 22_8
+15V_ALWP
PC80
.1u/50V_6
PR118
*200K_4
PR117
*39K_4
VIN
+15V
+5VPCU
PR111
1M_6
PR109
1M_6
S5D
PQ24
AO4496
+5V_S5
<30,37,38> S5_ON
PQ20
DTC144EUA
PR110
1M_6
PQ19
DMN601K-7
+5VPCU
MAIND
PQ47
AO4496
+5V
PC85
1u/25V_6
+3VPCU
MAIND
PQ22
AO4496
+3V
+3VPCU
S5D
PQ17
AO3404
+3V_S5
Quanta Computer Inc.
PROJECT : ZK6
Size
Document Number
SYSTEM 5V/3V (ISL6237)
Rev
1A
Date: Friday, April 24, 2009
Sheet 32 of 42



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PROJECT : ZK6

Size	Document Number	Rev
	CPU CORE(ISL6266A)	1A

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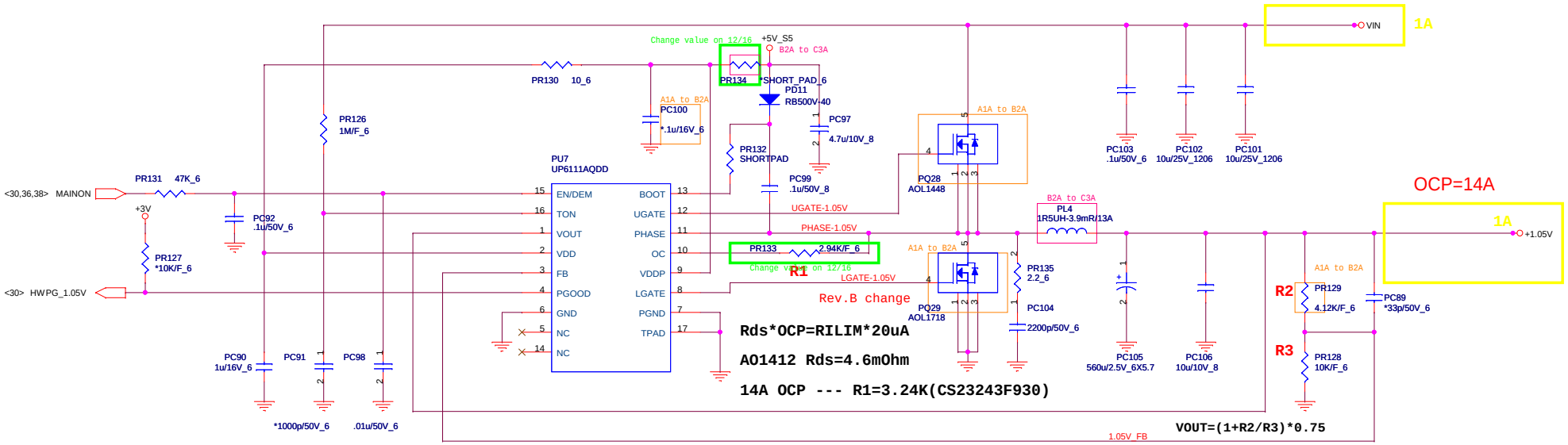

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

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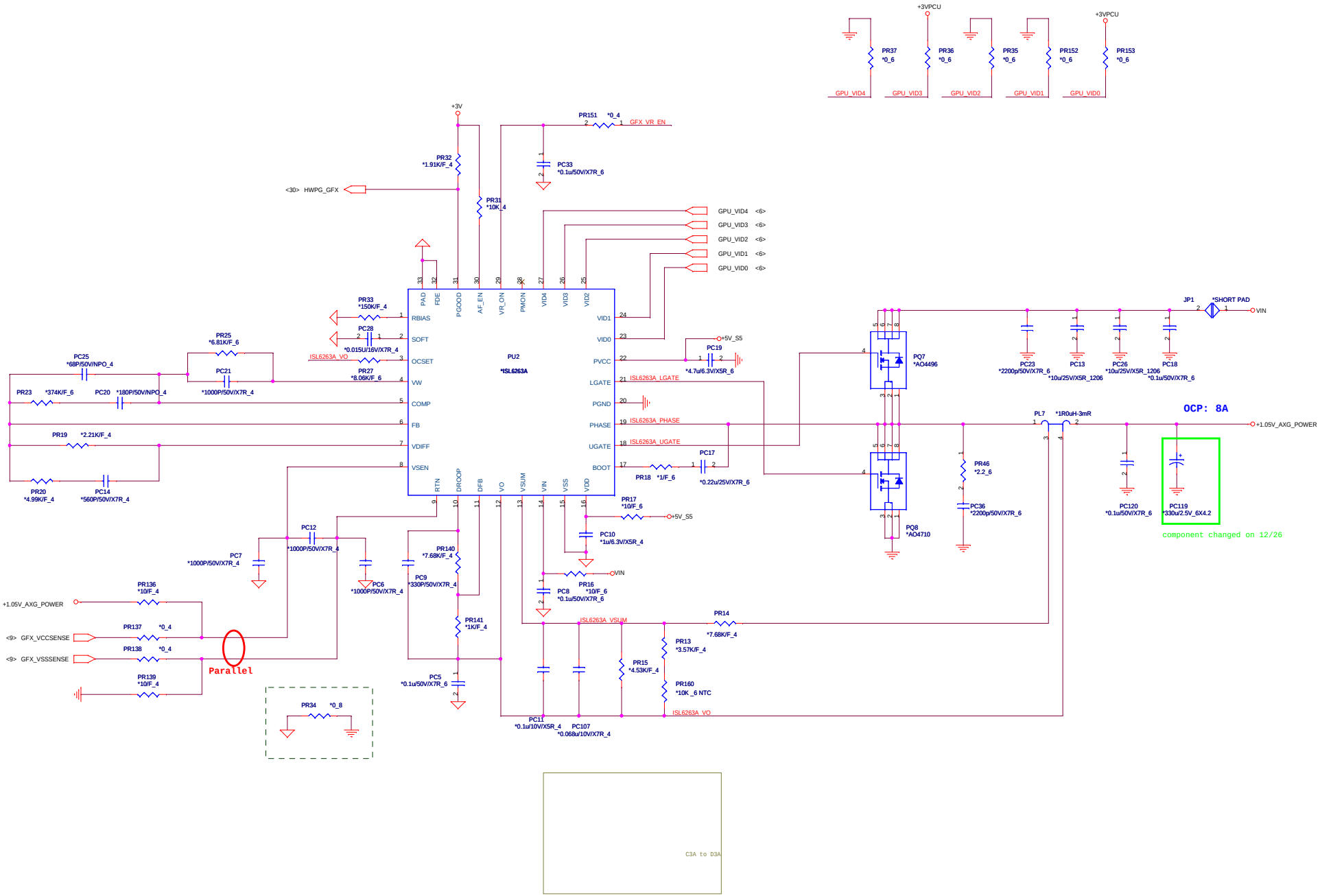
PROJECT : ZK6		
Size	Document Number	Rev
	VTT 1.05V (RT8202)	1A
Date: Friday, April 24, 2009	Sheet 34 of 42	

all component in this page would be stuff for UMA only



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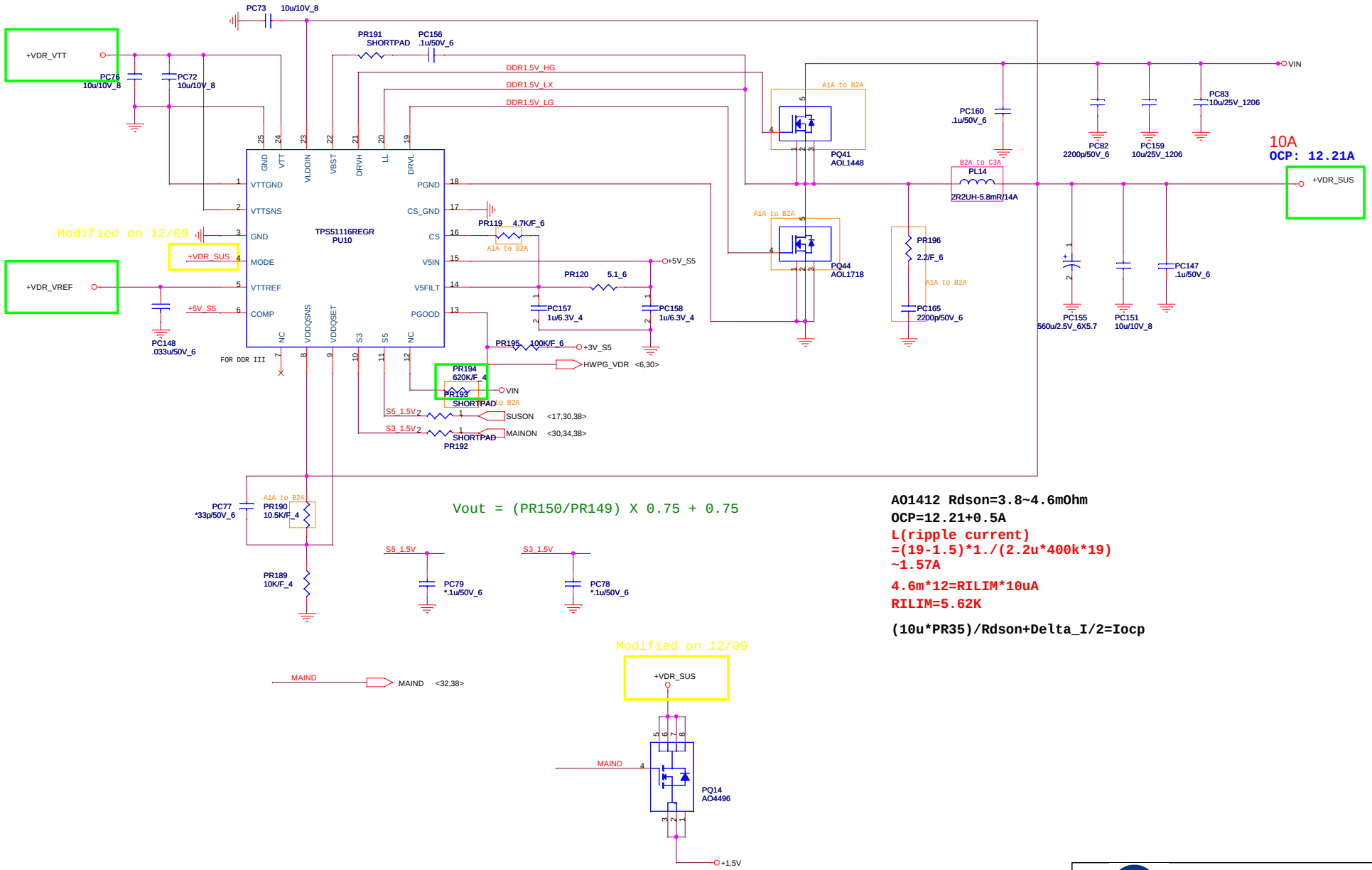
PROJECT : ZK6

Size	Document Number	Rev
	+1.05V_GFX-ISL6263A	1A

Date: Friday, April 24, 2009 Sheet 35 of 42



Vout = (PR150/PR149) X 0.75 + 0.75

AO1412 Rdson=3.8~4.6mOhm
OCP=12.21+0.5A
L(ripple current)
=(19-1.5)*1./(2.2u*400k*19)
~1.57A

4.6m*12=RILIM*10uA
RILIM=5.62K

(10u*PR35)/Rdson+Delta_I/2=Iocp

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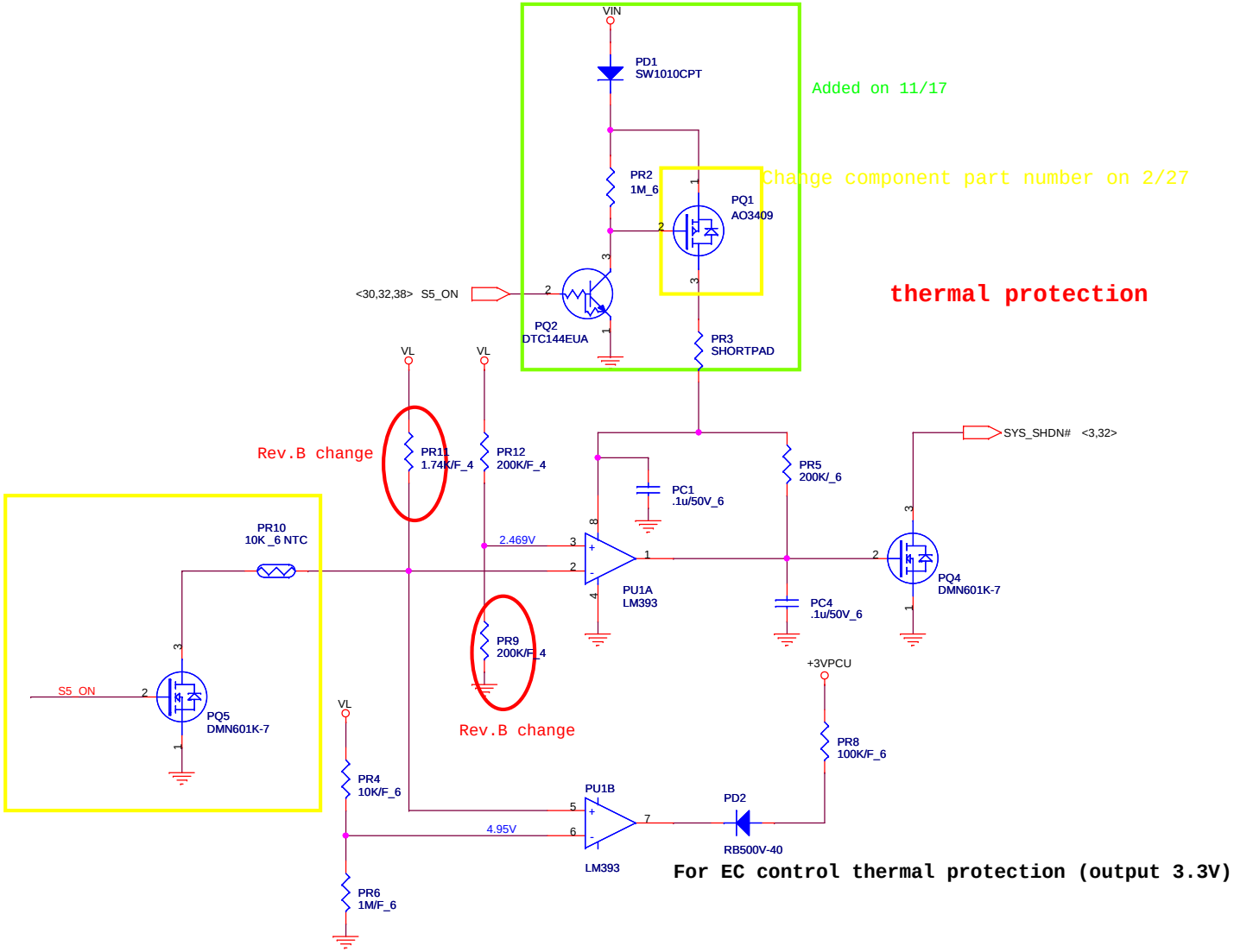
PROJECT : ZK6

Size	Document Number	Rev
	DDR 1.8V(TPS51116)	1A

Date: Friday, April 24, 2009 Sheet 36 of 42



Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	Thermal protect	1A

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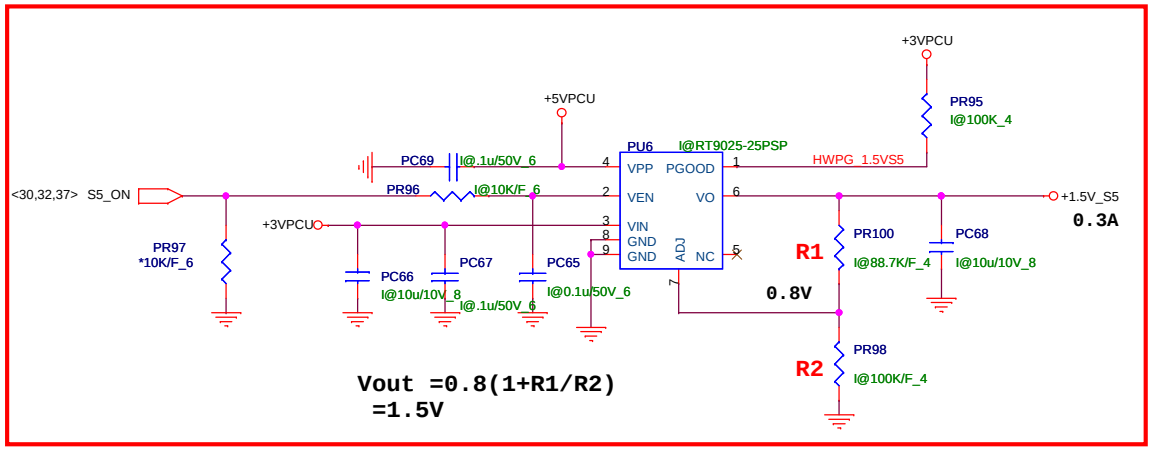

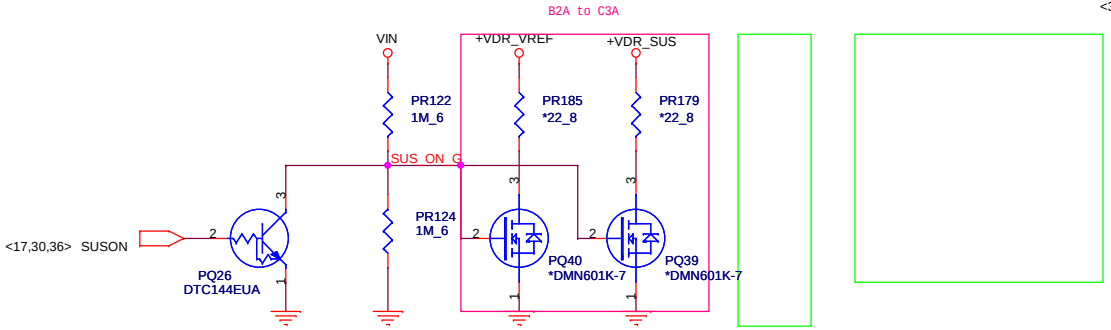

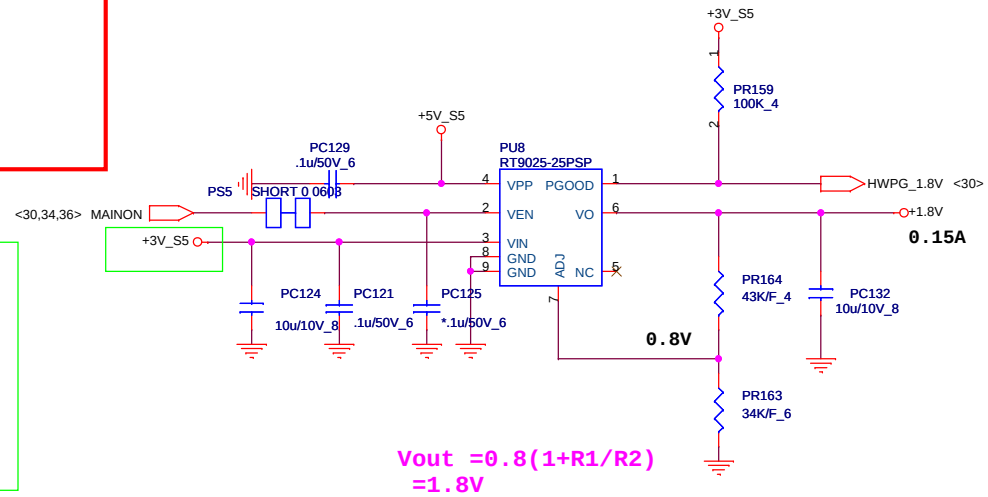

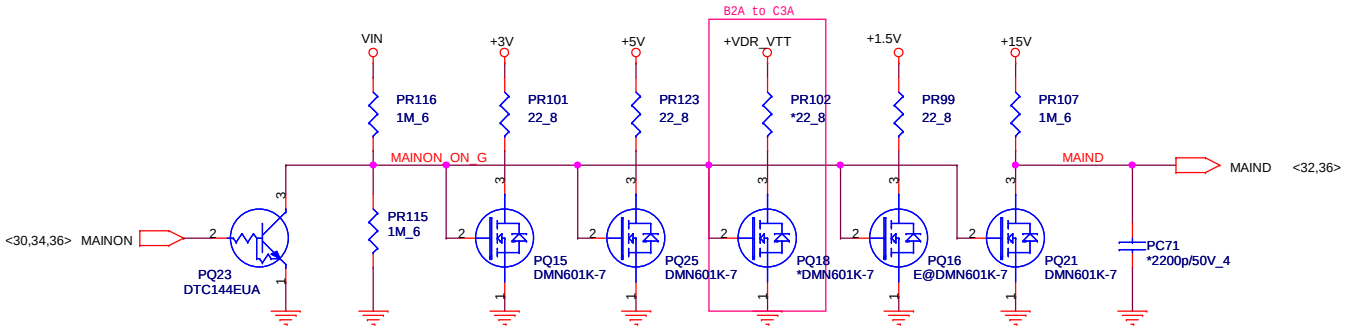

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PROJECT : ZK6

Size	Document Number	Rev
	Discharge (2.5V/1.5V)	1A

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